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MS-7A59

Intel -Kabylake plamform Z270

ATX

Ver: 11

CPU:

kabylake-S

System Chipset:

Z270

Onboard Chip:

HD Audio Codec:ALC1220

LAN:INTEL I219

SIO:Nuvoton 6795

Flash ROM: SPI 128MB

Main Memory:

DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)

ACPI:

NIKO/UPI

PWM:

UPI9508

Expansion Slots:

PCI Express (X16) Slot *1

PCI Express (X8) Slot *1

PCI Express (X4) Slot * 1

PCI Express (X1) Slot * 3

M2 * 3

Other:

SATA3.0 x6 (PCH)

FRONT USB2.0 *4

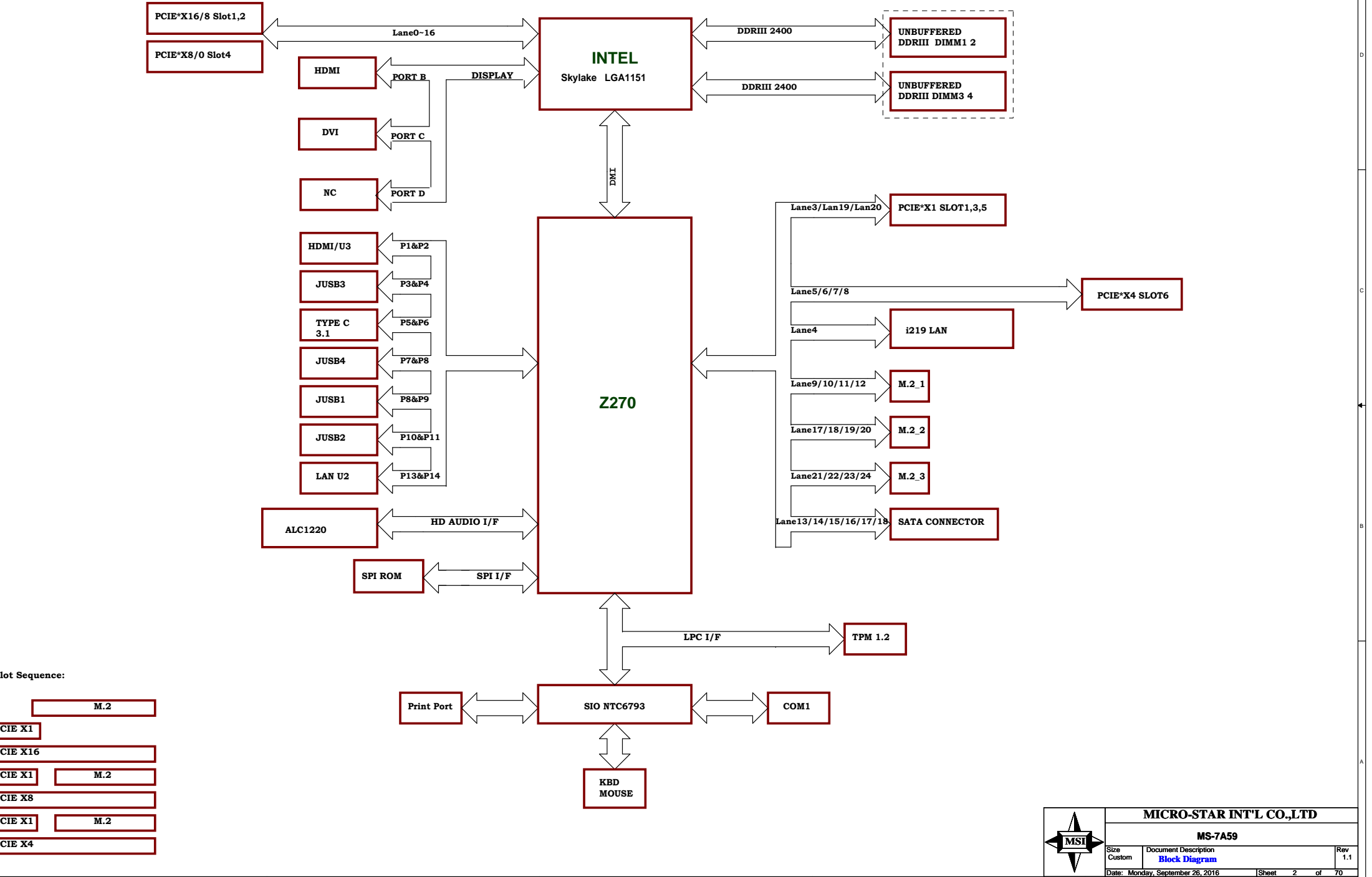
FRONTUSB3.0 *4

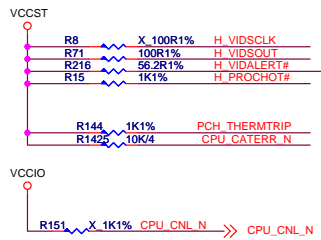
REAR USB3.0 *2

REAR USB2.0 *2

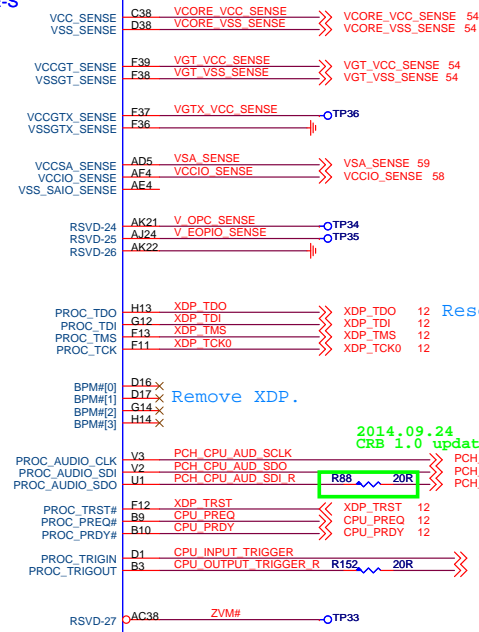
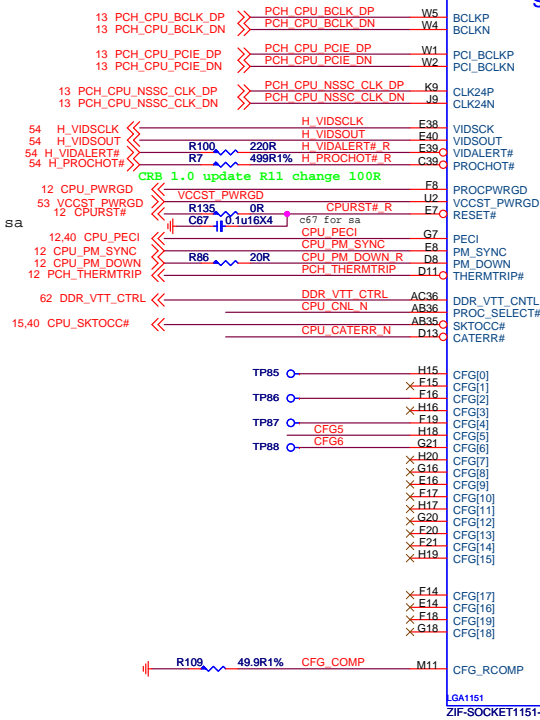
REAR USB TYPE A+C

MS-7A59 Block Diagram



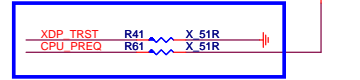
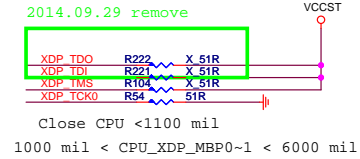


CPURST#_R. need save 0.1u mlcc. for sa



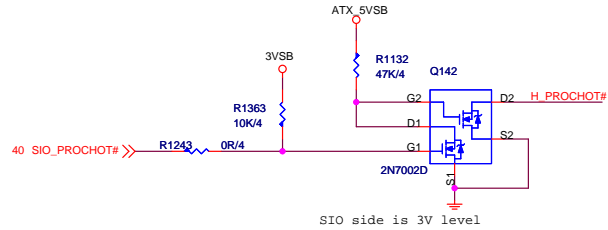
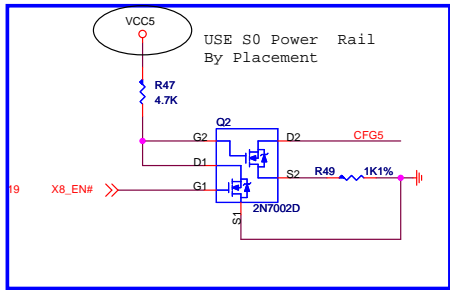
Reserve for DCI.

2014.09.24 CRB 1.0 update R29 change 20R



X8 Ctrl

ENABLE#	SLOT1	SLOT4
X8		
0	X8	X8
1	X16	X0



CFG Strap

CFG Table

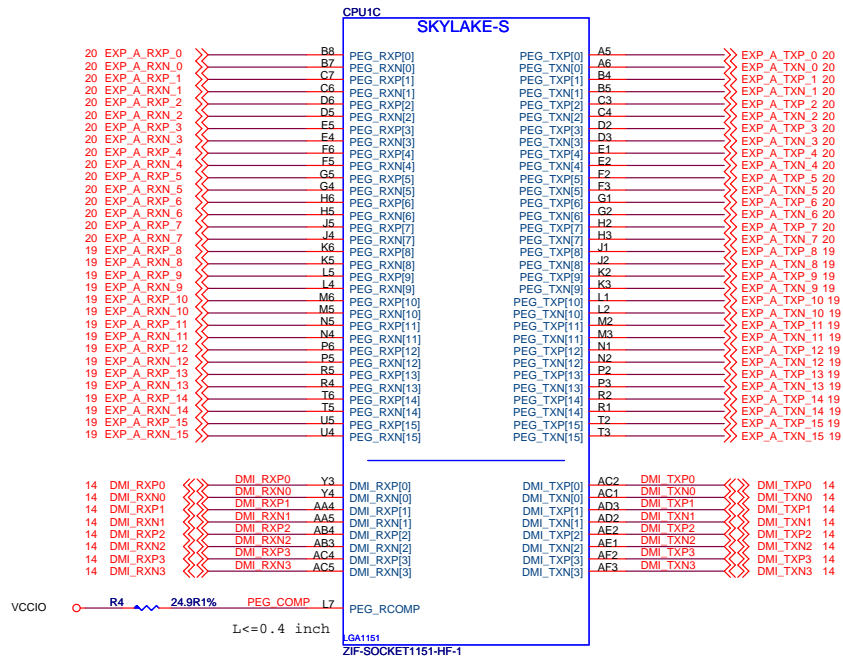
	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

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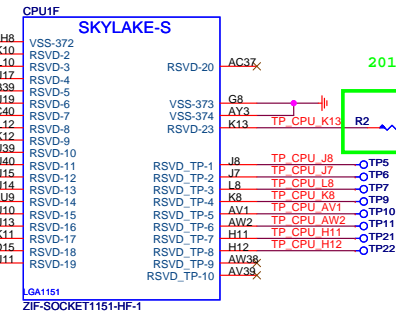
Size Custom Document Description CPU-Control/MISC/CFG/Audio Rev 1.1

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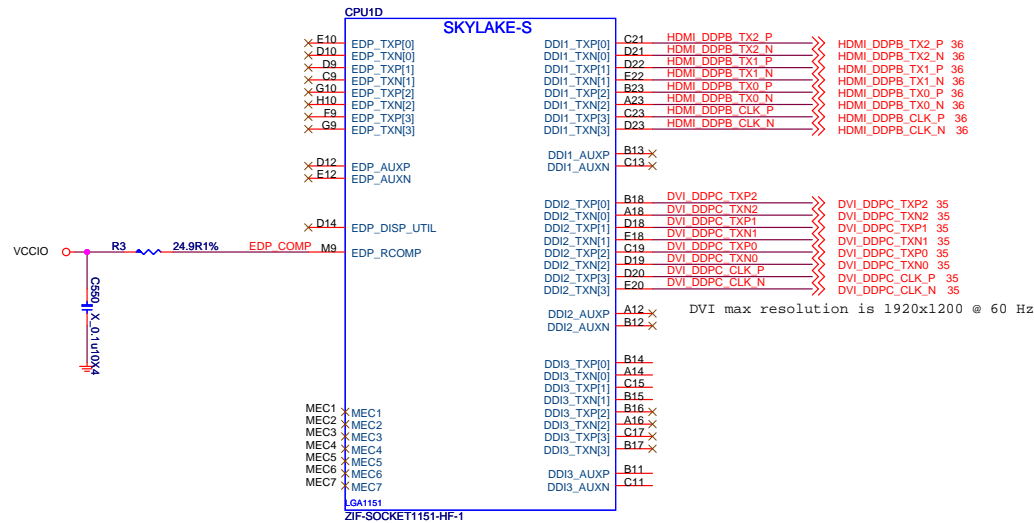


CRB 1.0 update
TP37
For Test

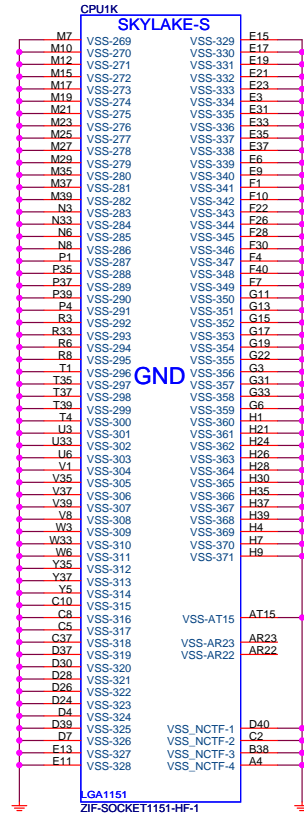
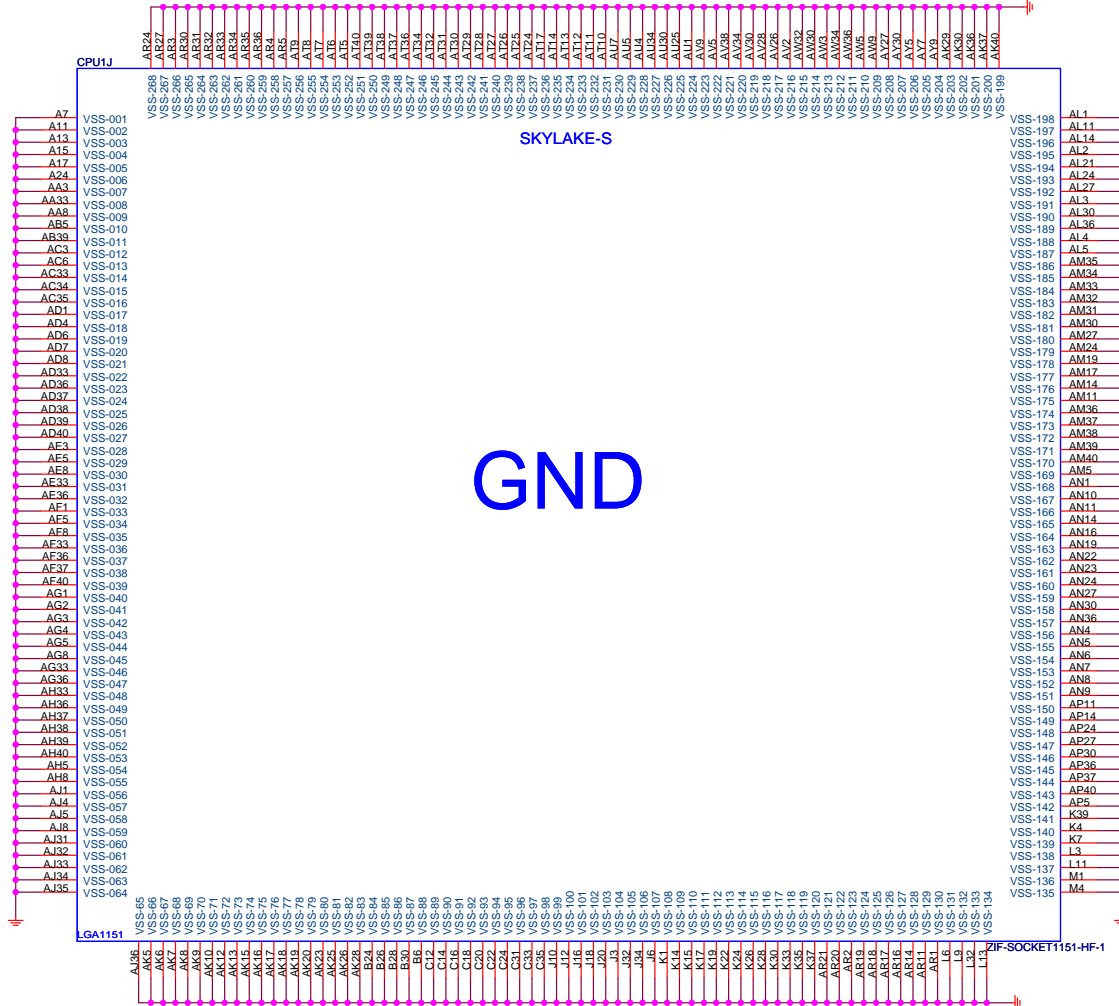
2014.09.24



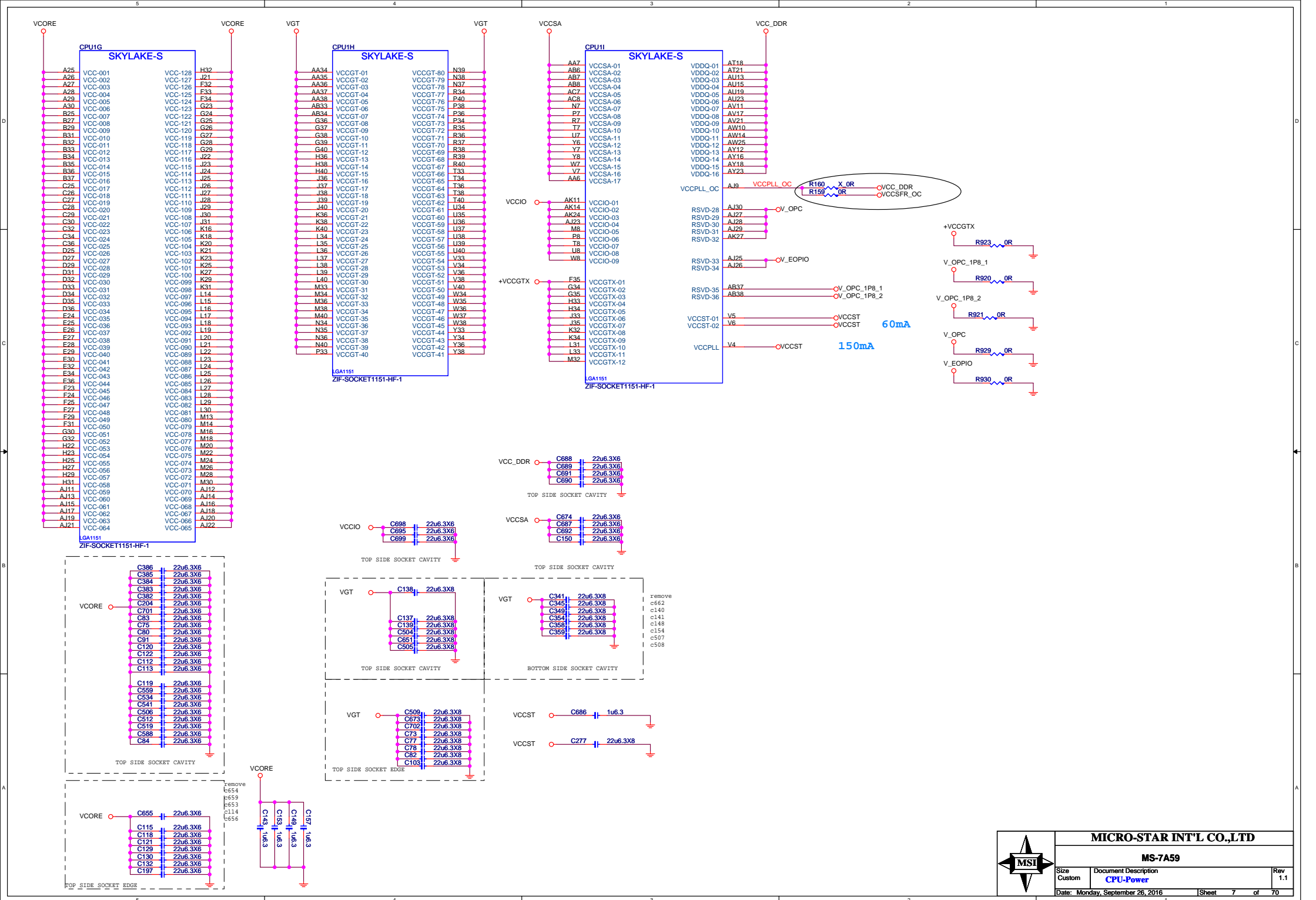
CRB 1.0 update
CRB unstuff
PCB come back remove

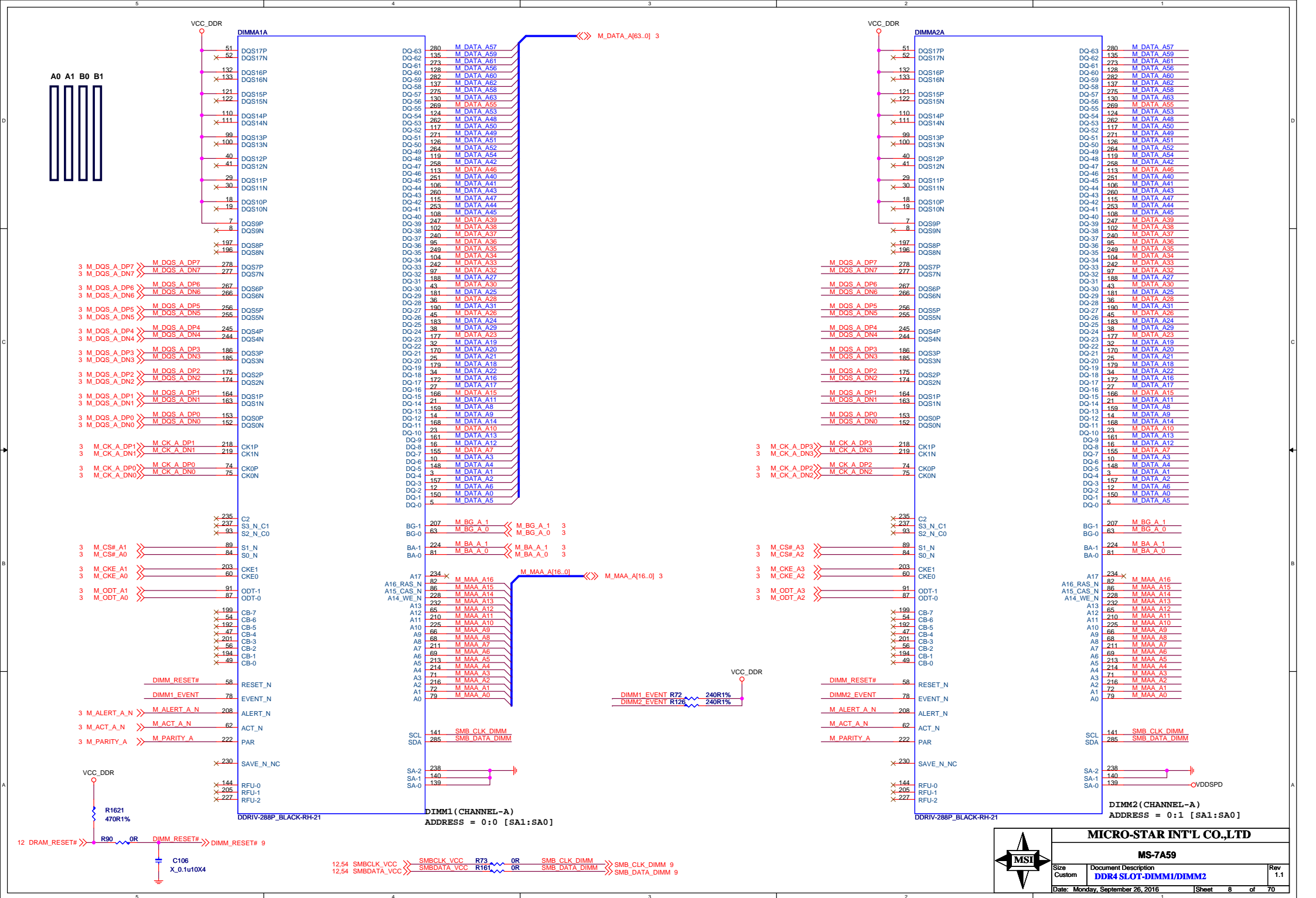


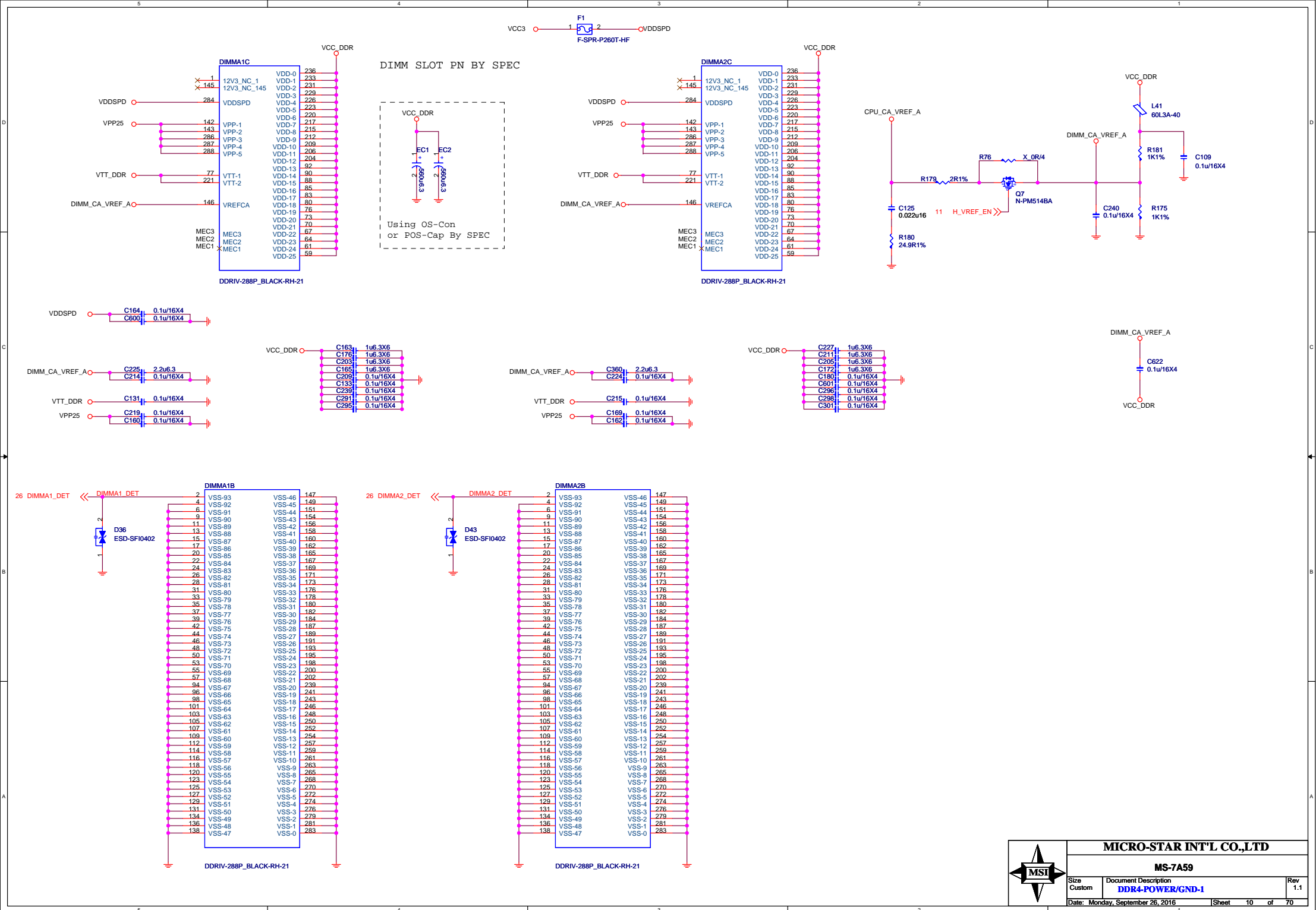
GND

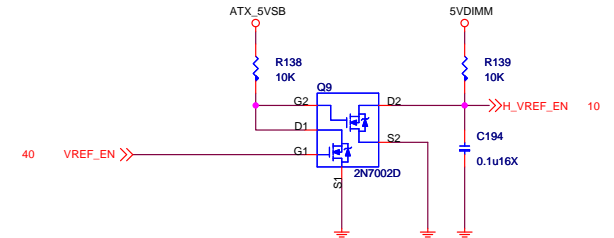
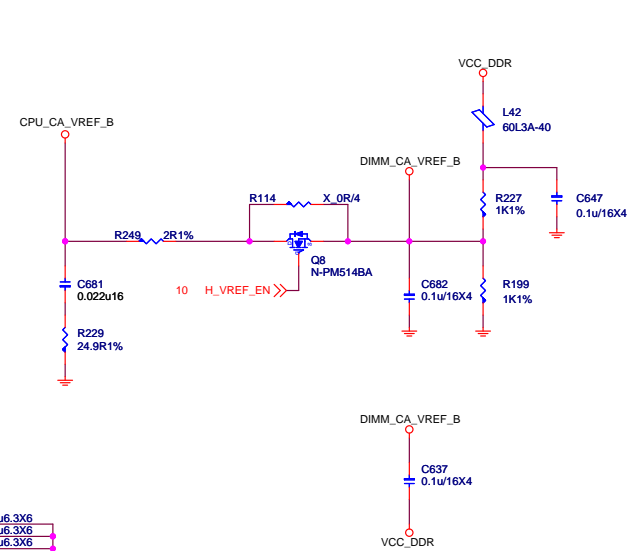
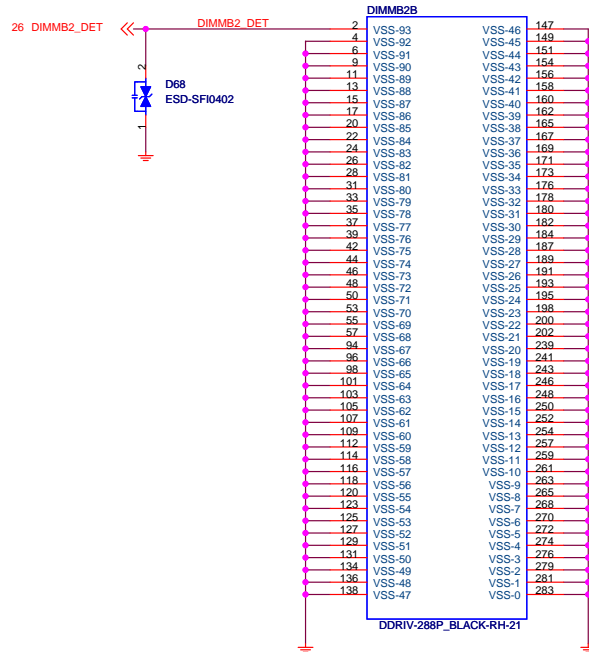
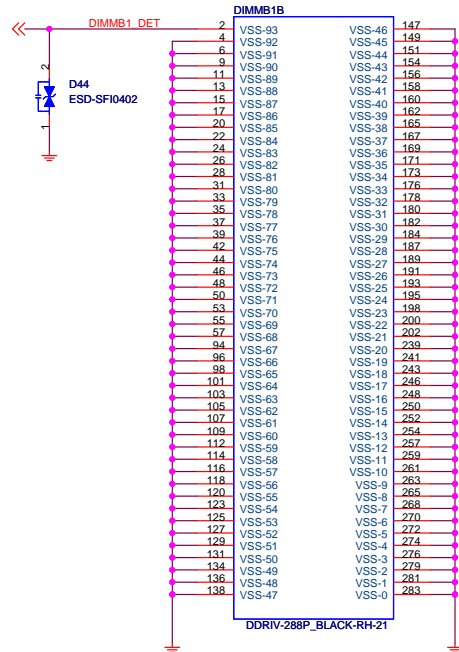


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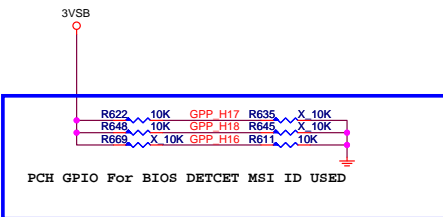




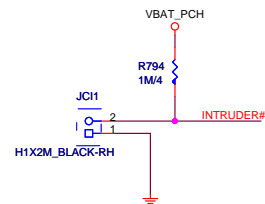
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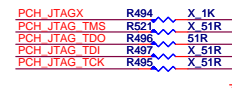
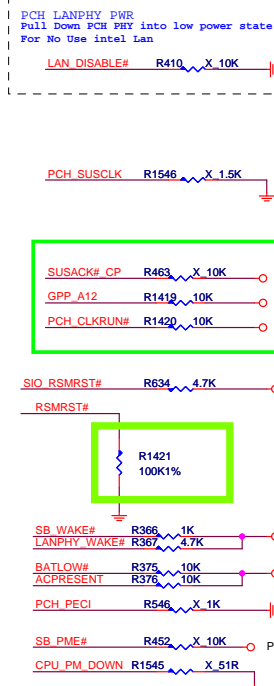
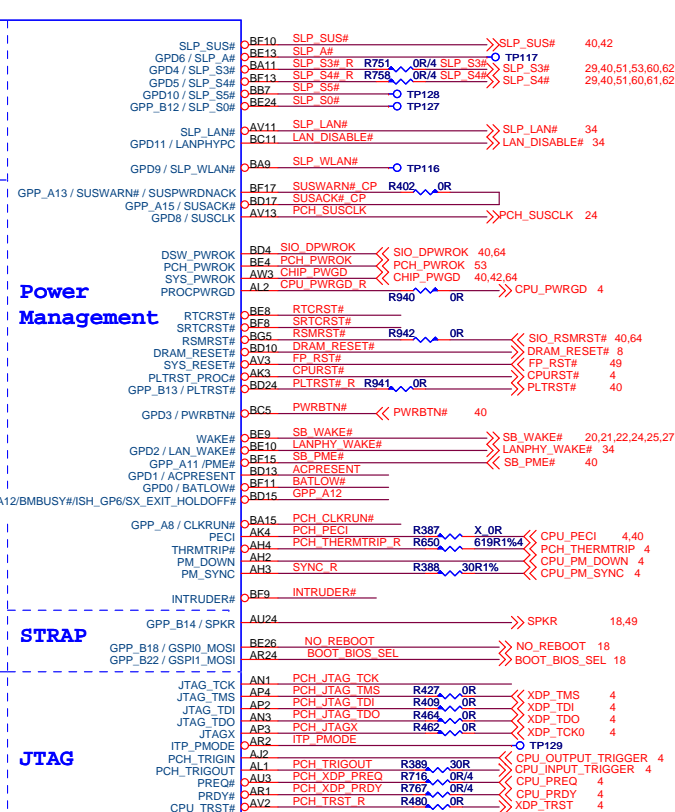
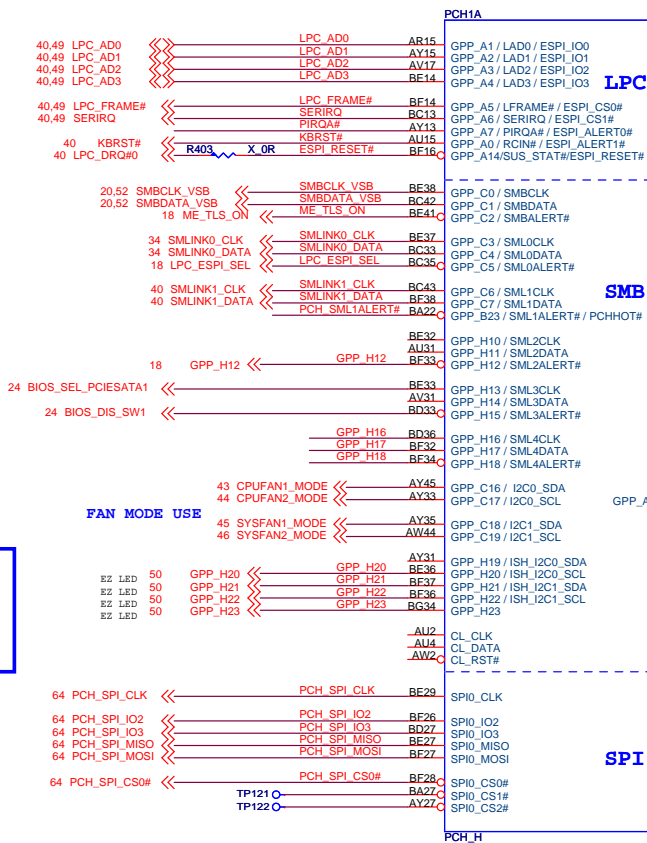
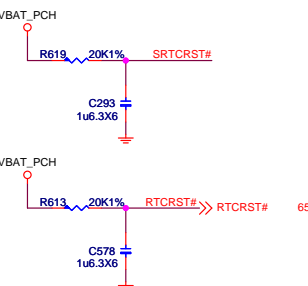
Size Custom	Document Description DDR4-POWER/GND-2	Rev 1.1
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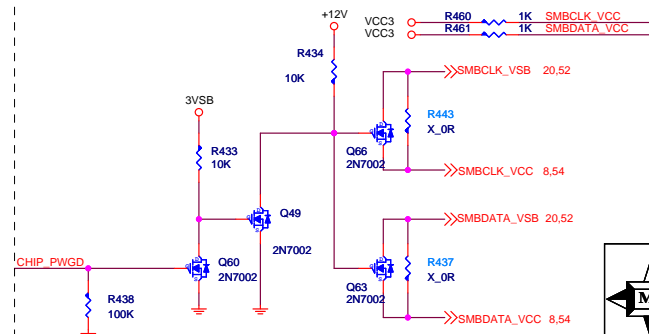
Chassis Intrusion



RTC



擺在一起(注意到所有的SMBUS的分枝)

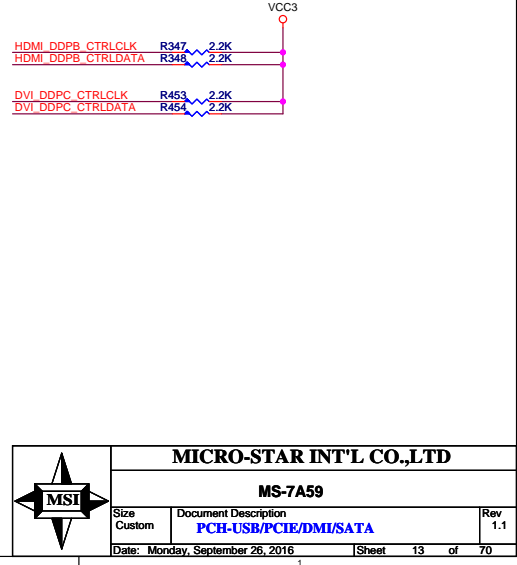
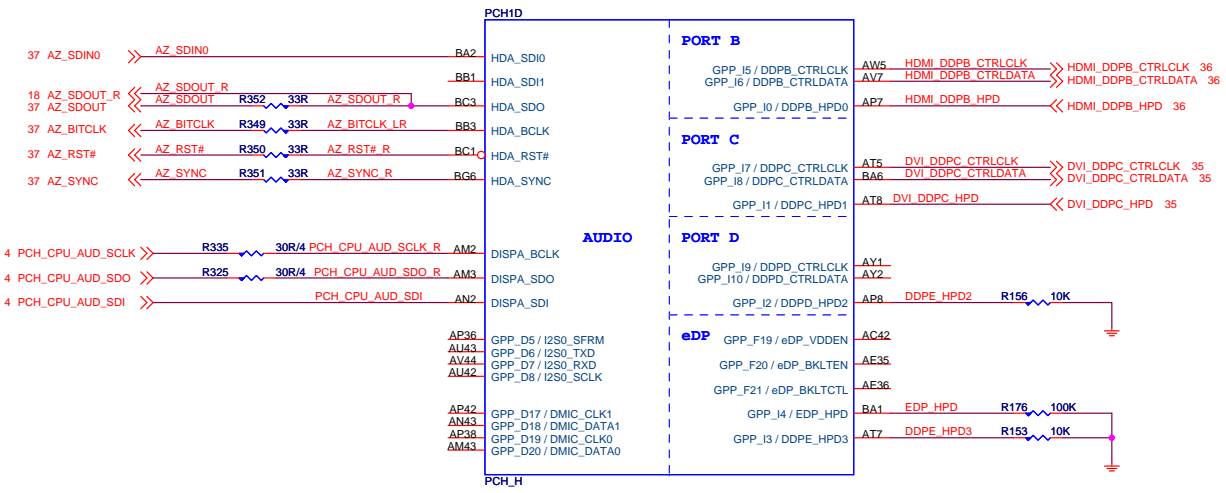
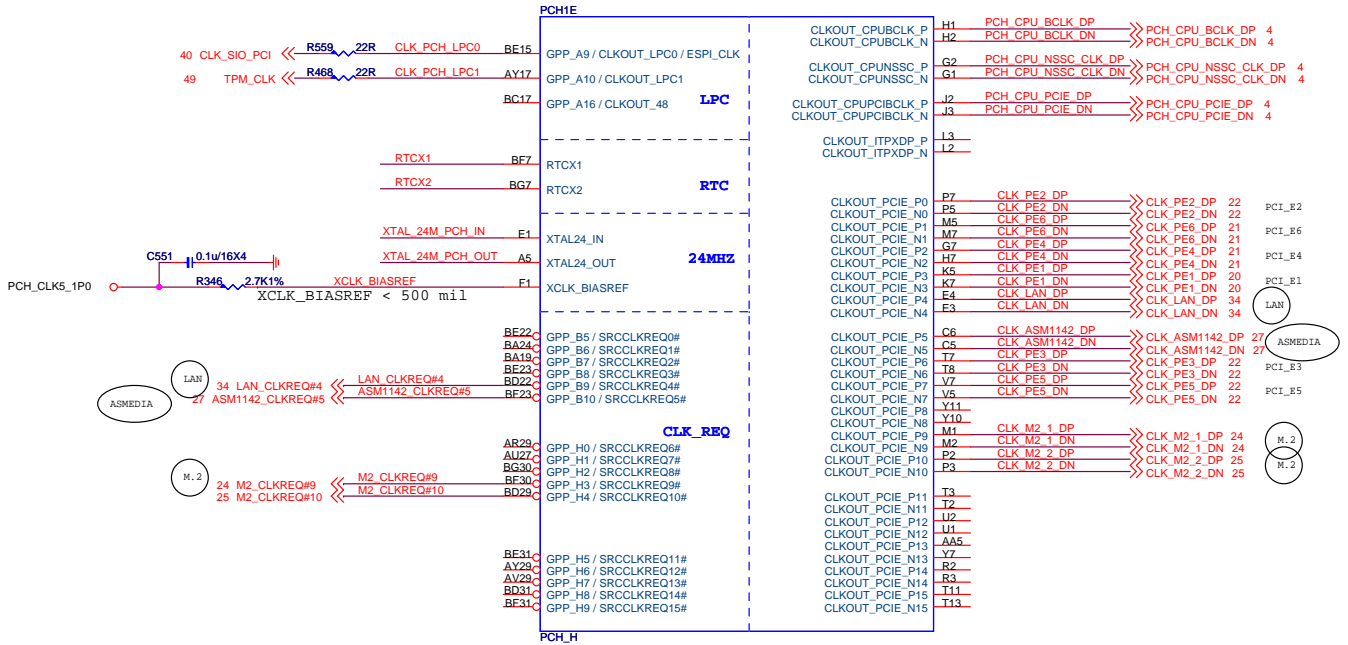
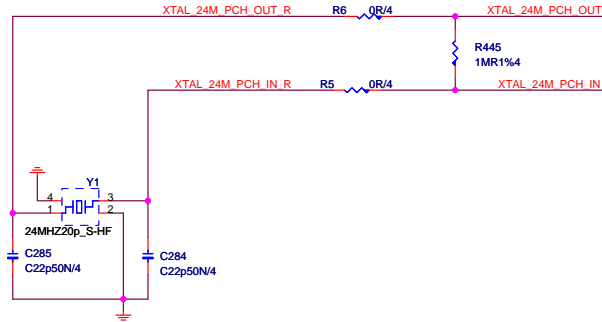
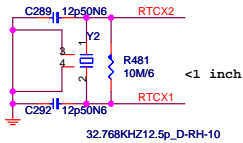


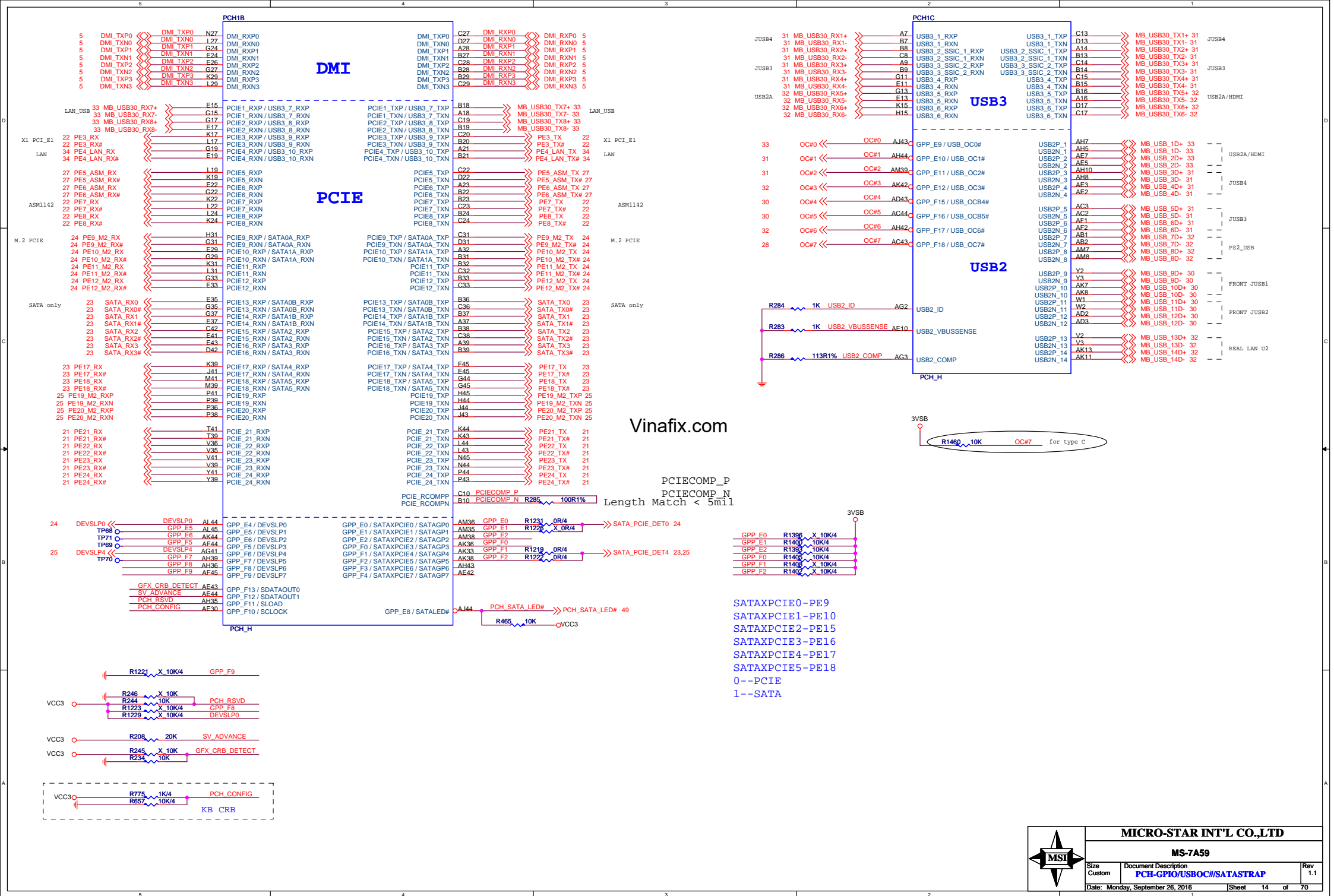
MICRO-STAR INT'L CO.,LTD			
MS-7A59			
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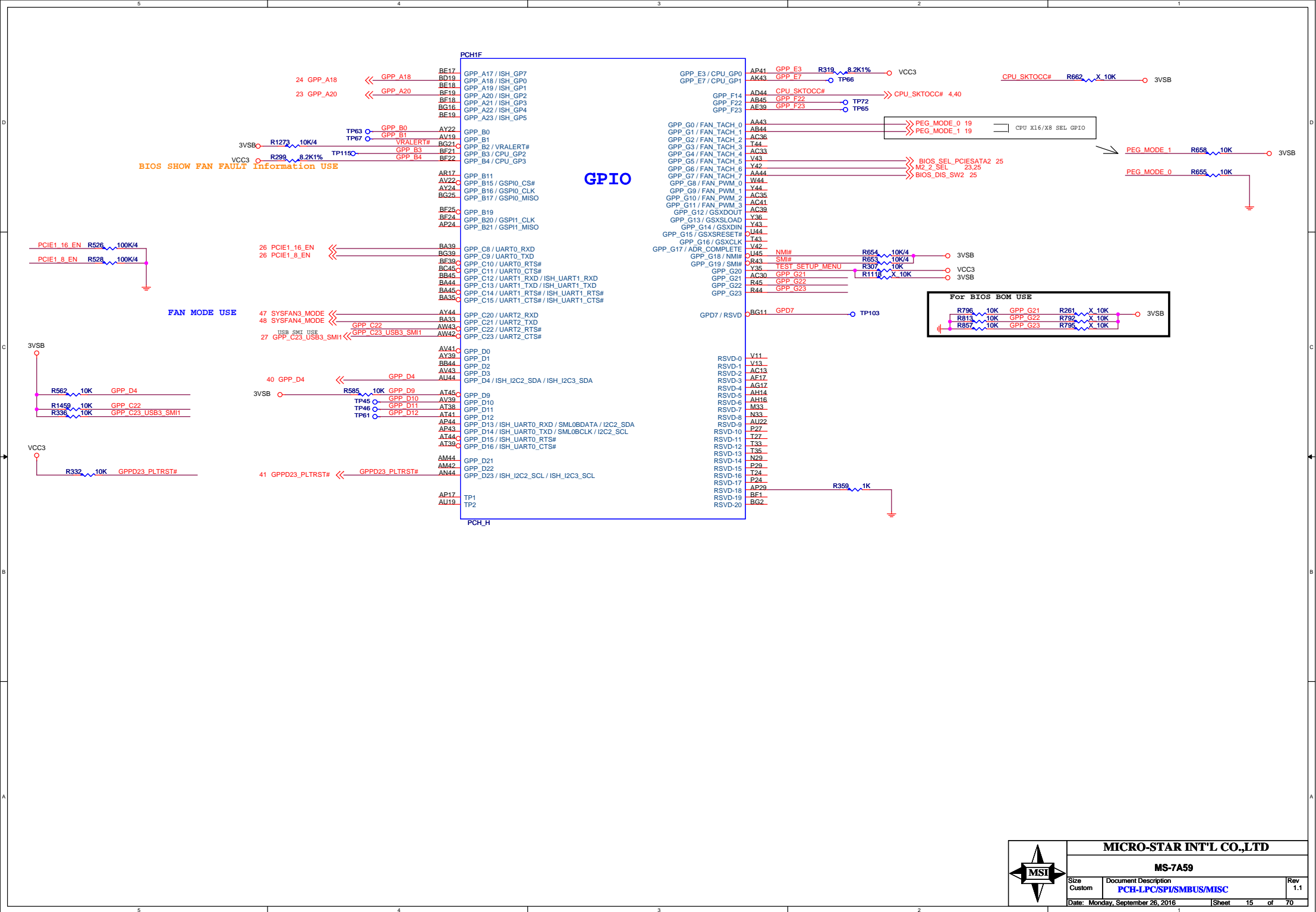
PCH_CLK

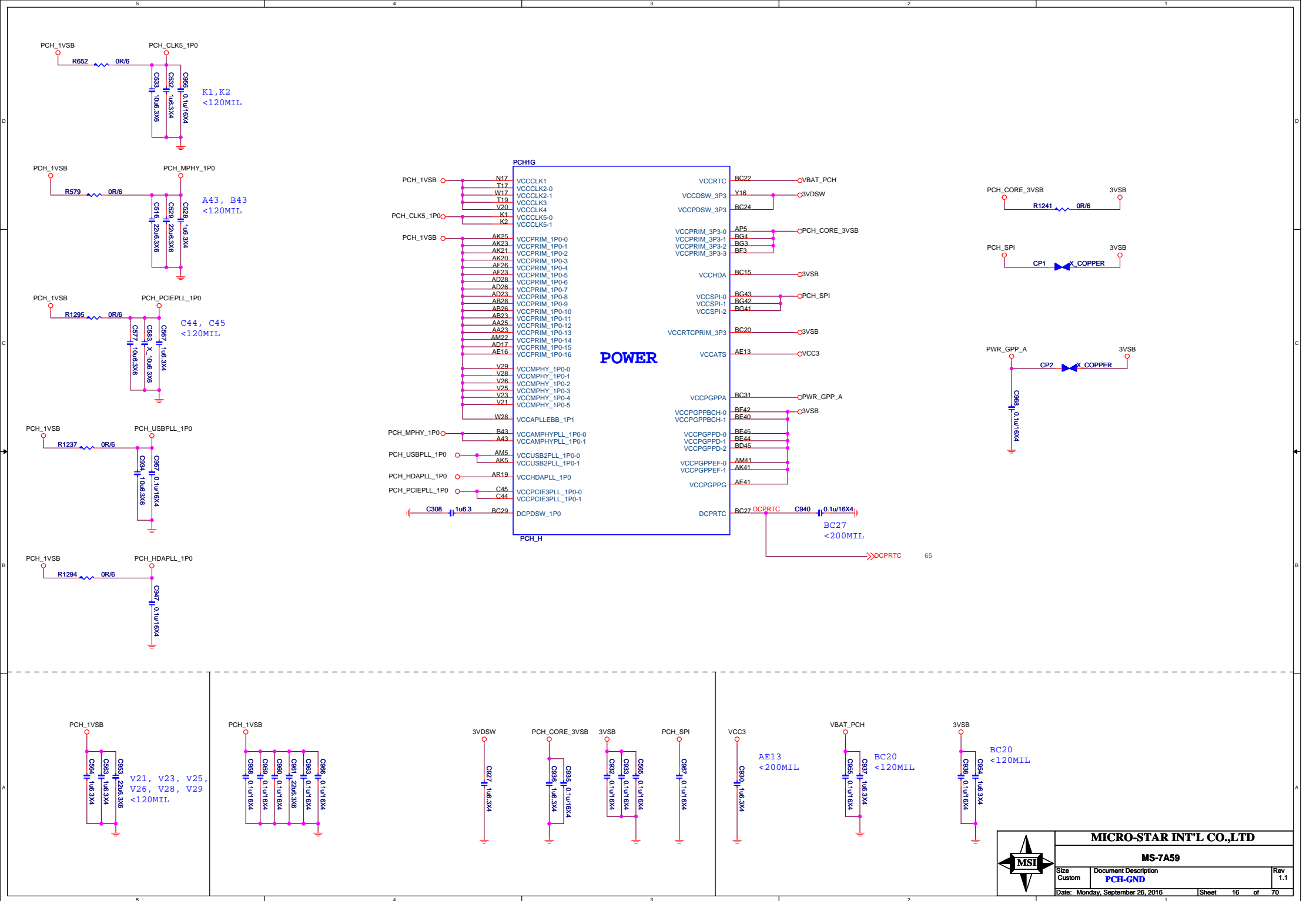
RTC Block

Close to PCH

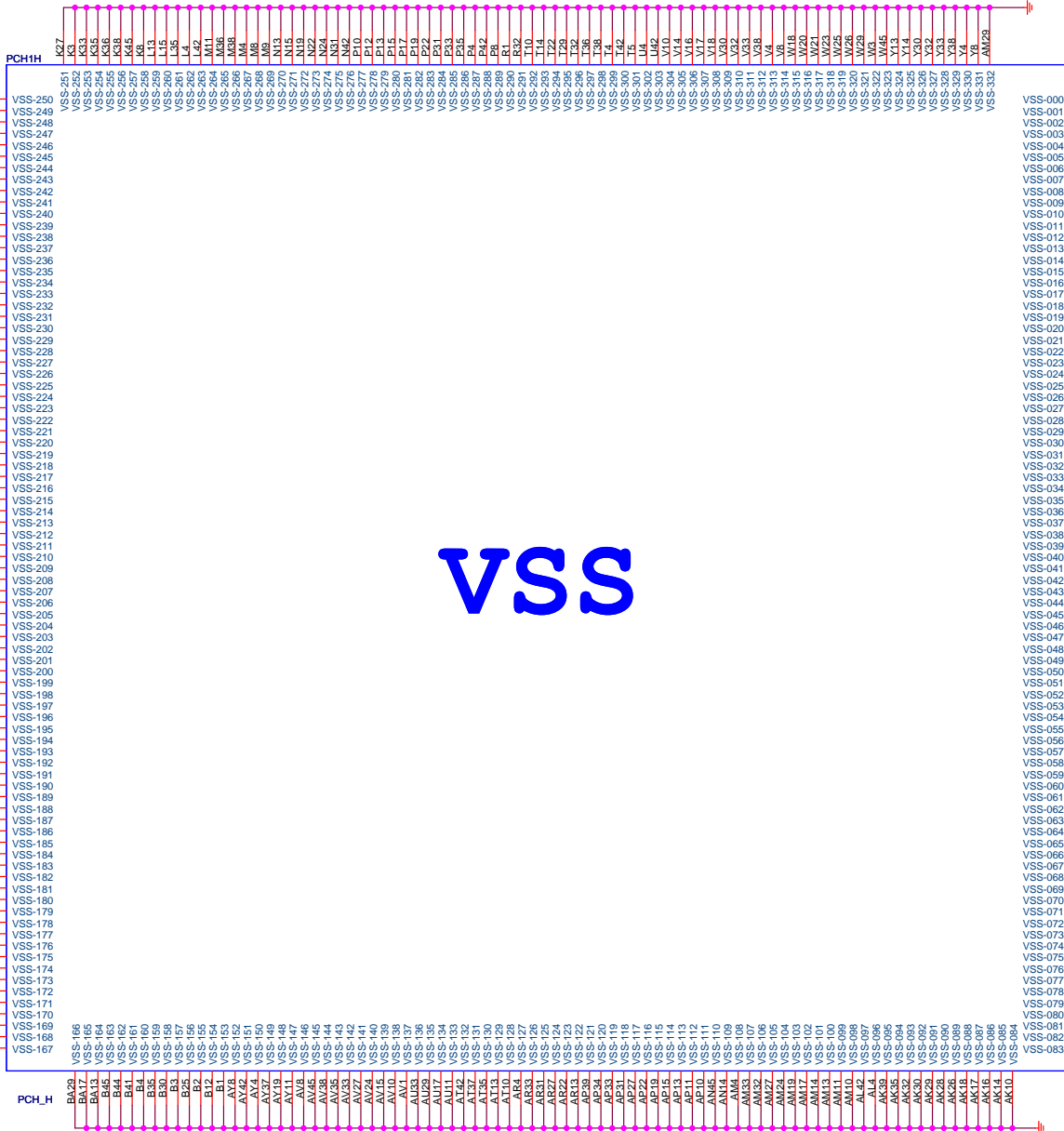




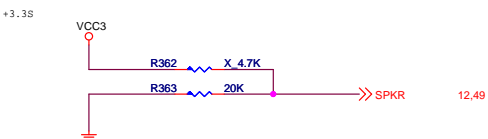




VSS

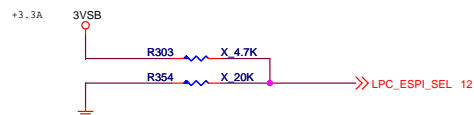


TOP Swap



Internal pull-down is disabled after PLTRST#

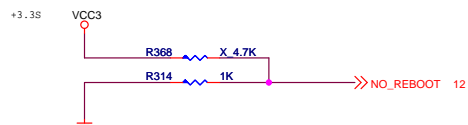
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

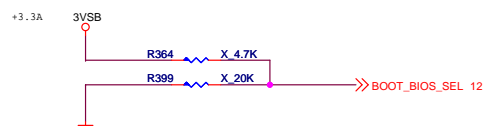
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

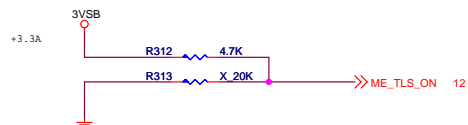
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

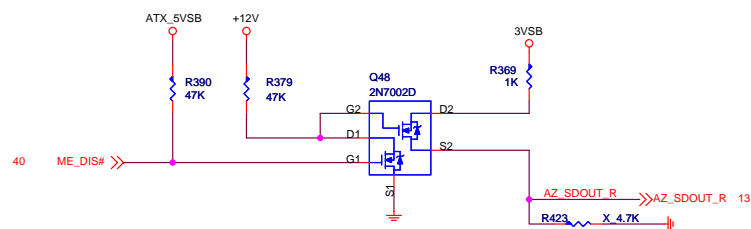
AMT and SBA with confidentiality



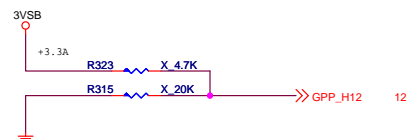
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE

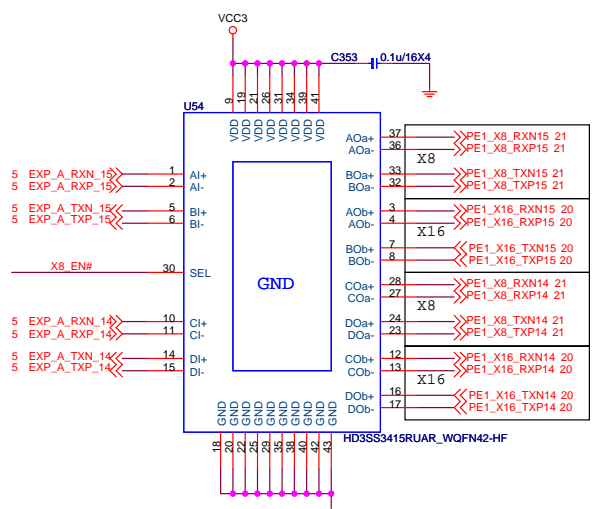
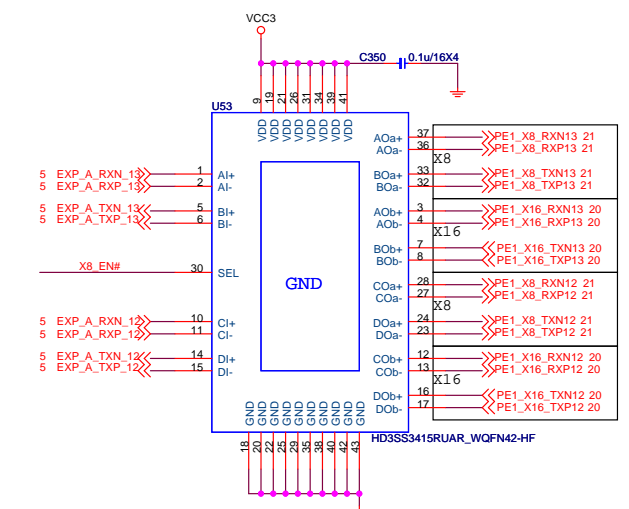
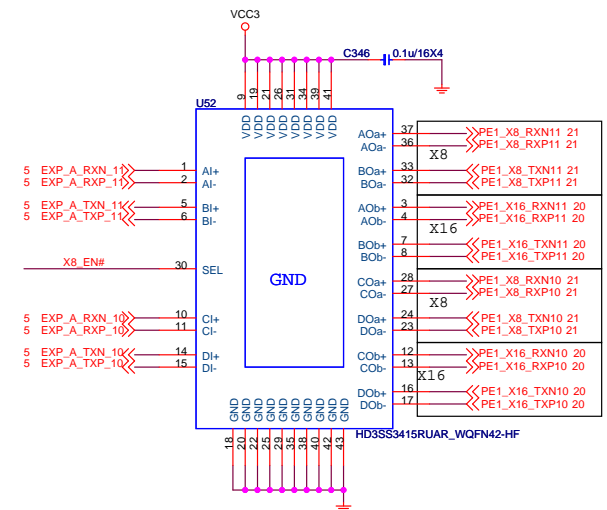
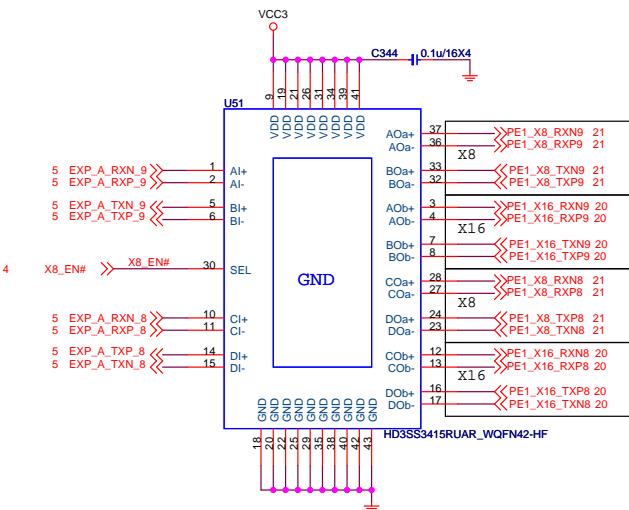


0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

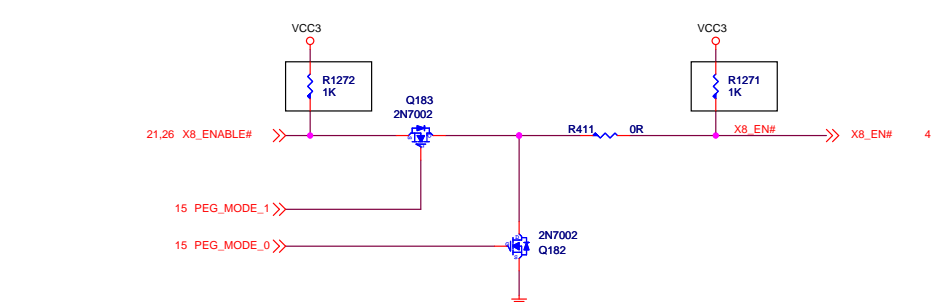
Internal pull-down is disabled after RSMRST



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MODE_1

0: BIOS MODE
1: HW MODE (Default)

HW MODE

PCH Status	MODE_0	MODE_1
AUTO	0	1

If USE HW MODE
GPP_G0 & GPP_G1 programming to GPI

If USE BIOS MODE
GPP_G0 & GPP_G1 programming to GPO

BIOS MODE

PCH Status	MODE_0	MODE_1
16,0	0	0
8,8	1	0

MODE_1/3

0: BIOS MODE
1: HW MODE (Default)

HW MODE

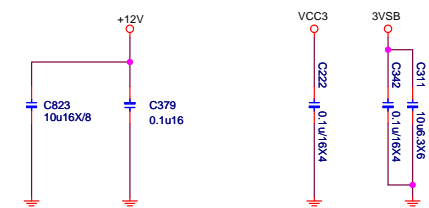
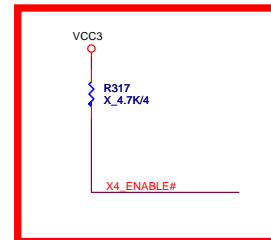
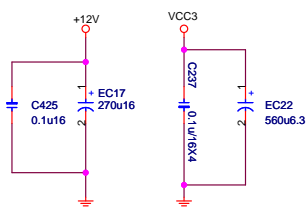
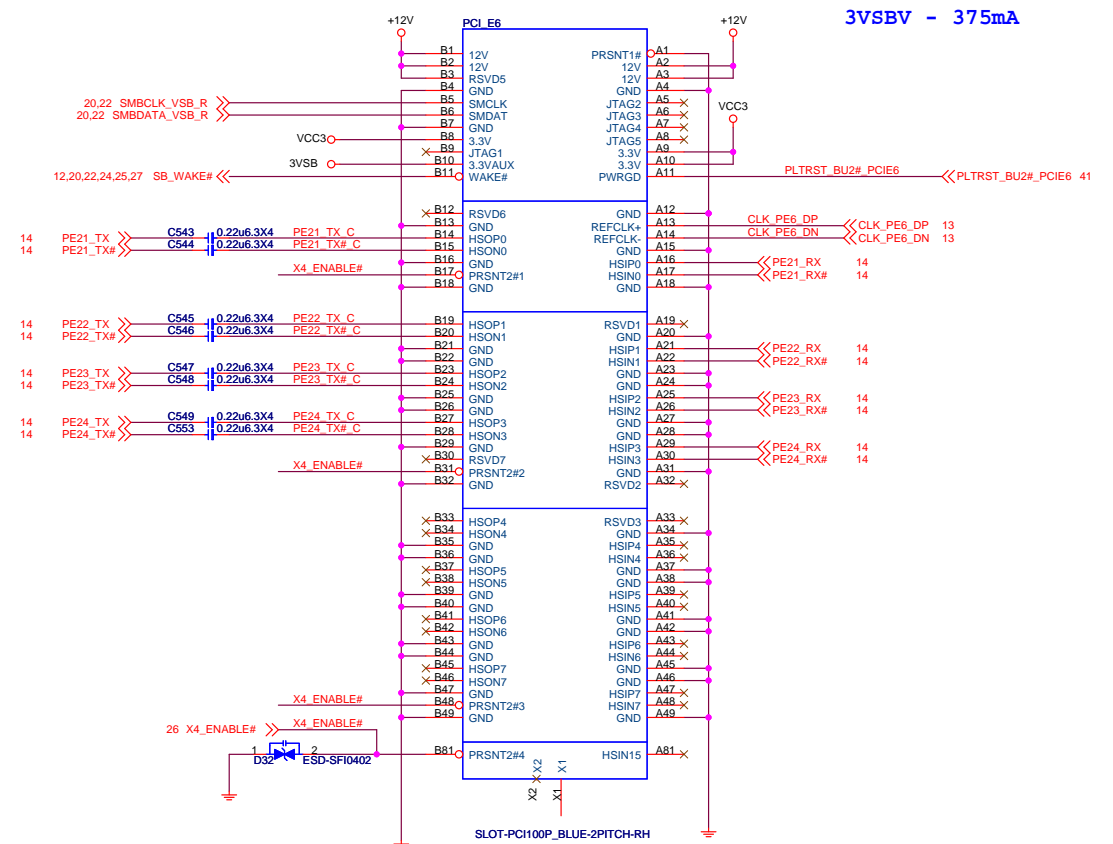
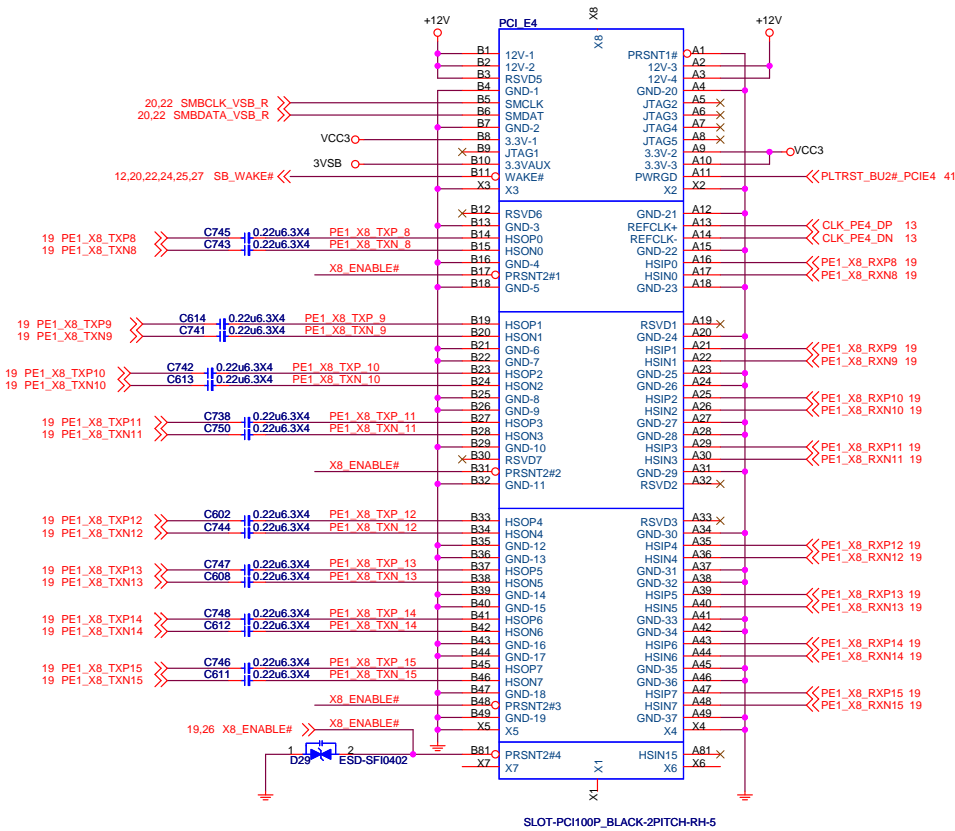
PCH Status	MODE_0/2	MODE_1
AUTO	0	1

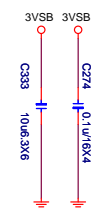
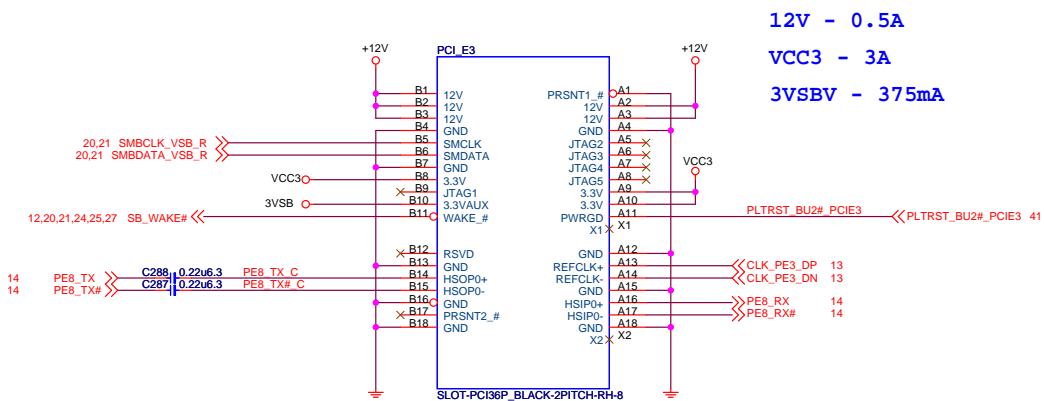
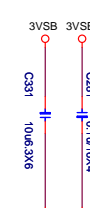
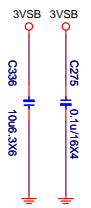
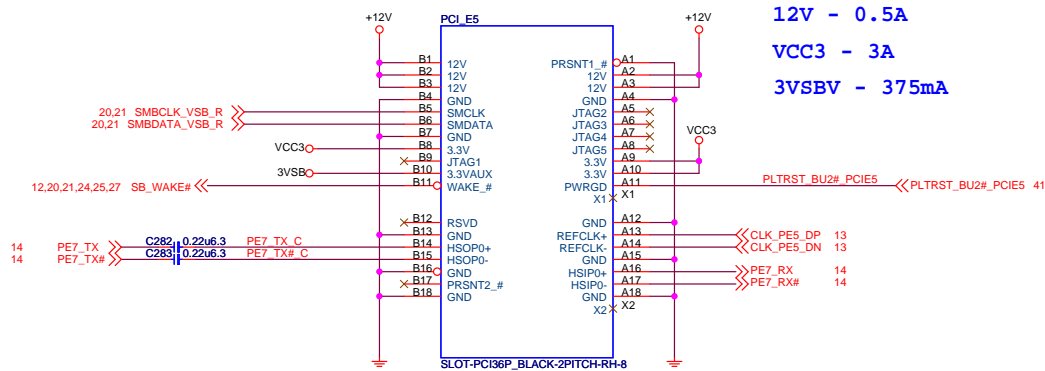
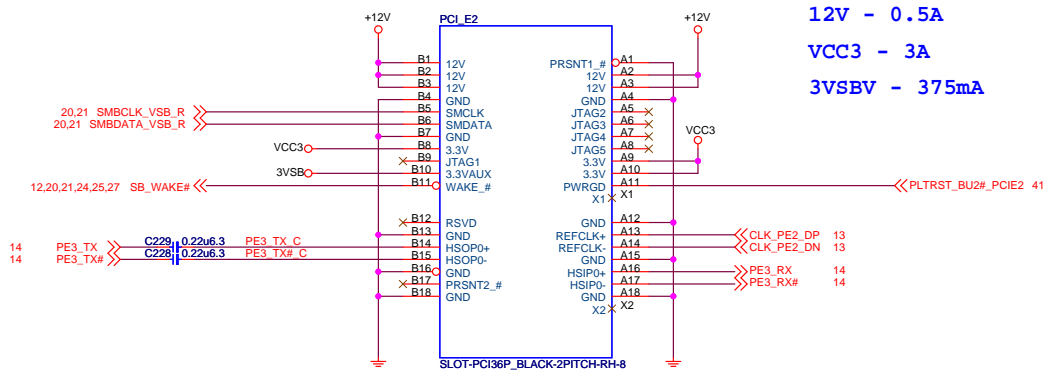


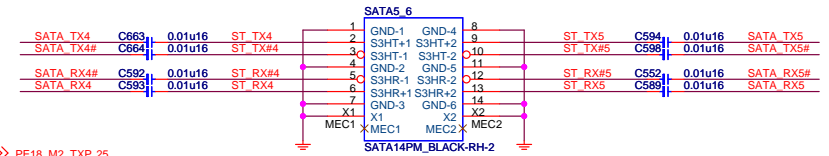
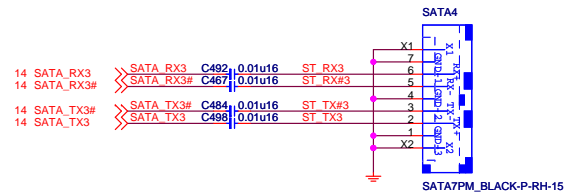
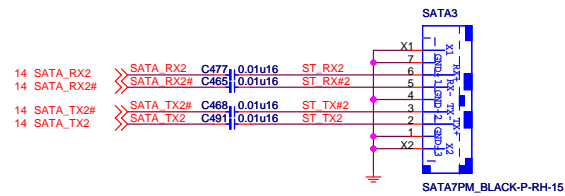
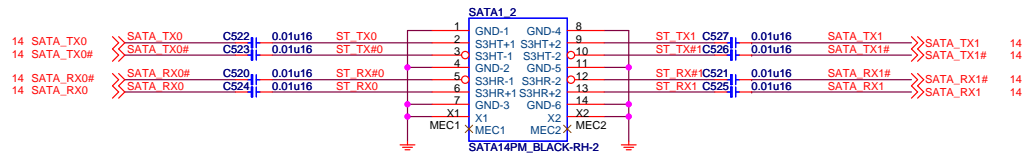
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PCI_Express X4 Slot

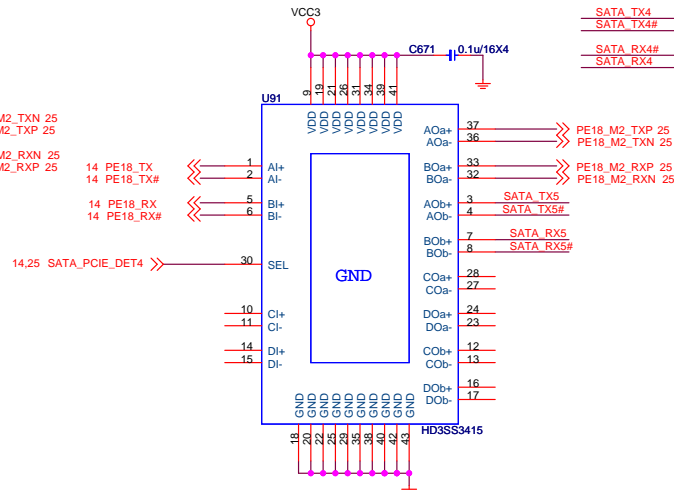
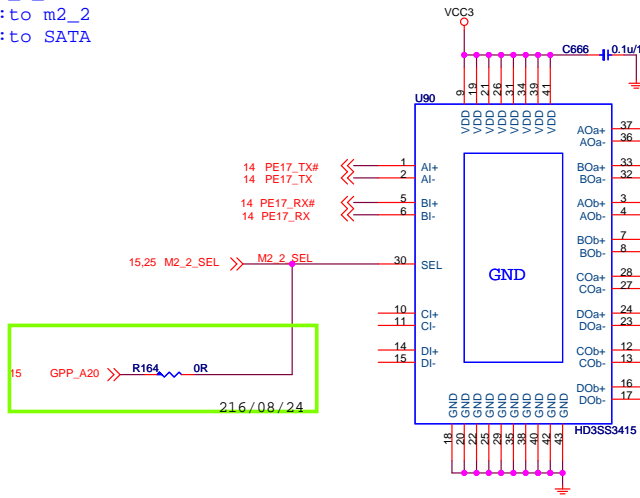
12V - 2.1A
VCC3 - 3A
3VSBV - 375mA

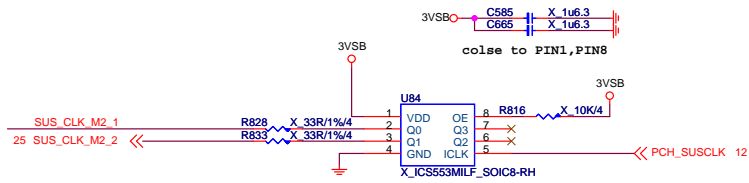


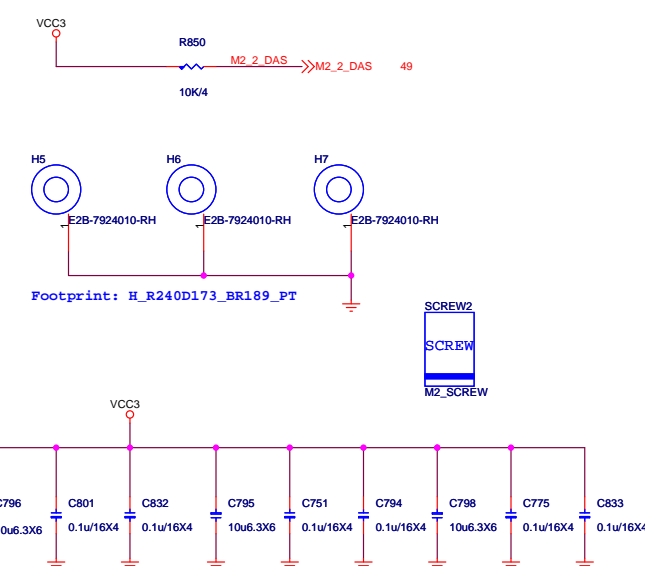
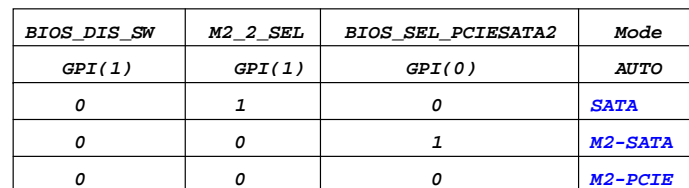




M2_2_SEL
0:to m2_2
1:to SATA

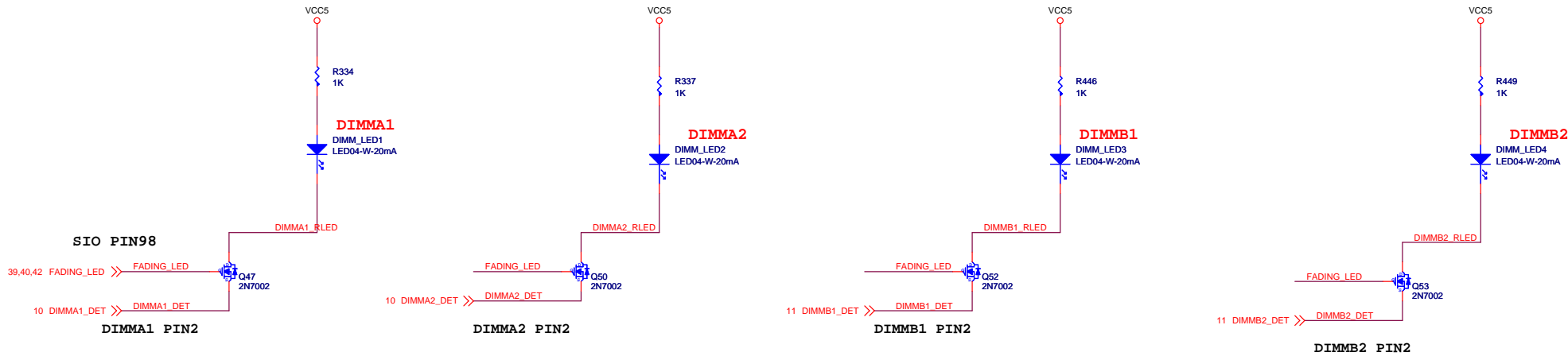






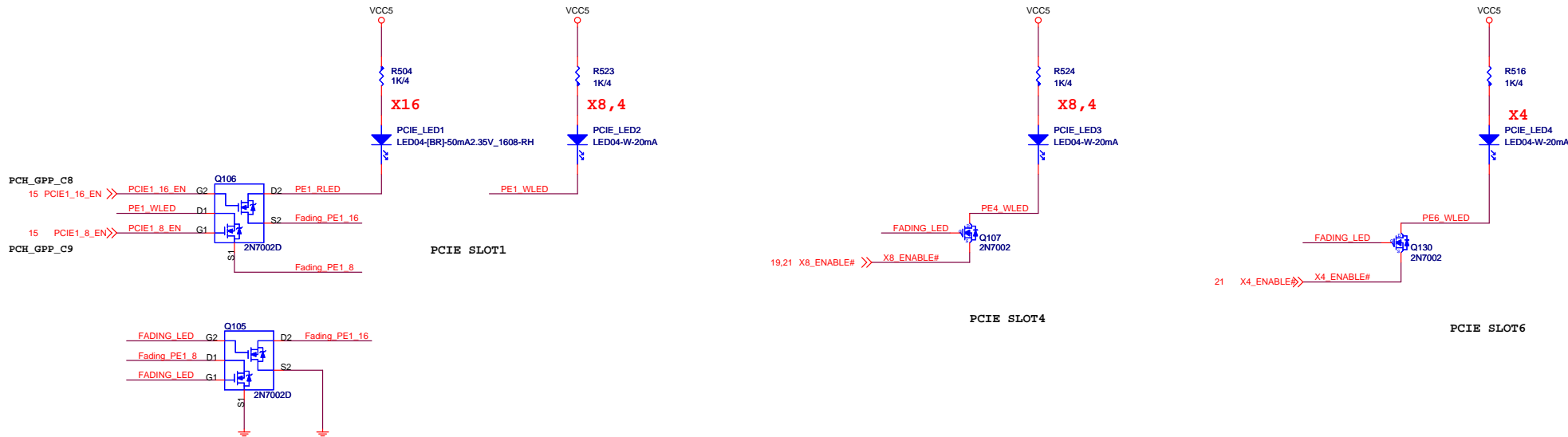
DIMM_SLOT

KRAIT GAMING LED >>WHITE:DOC-040S200-E07



LED 命名請以DIMM_LEDn n為數字

PCIE_SLOT_LED



Minimum gap should be greater of
>15mil with other signal.

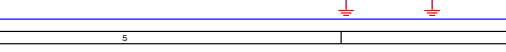
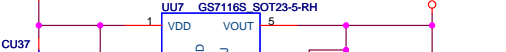
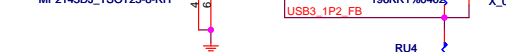
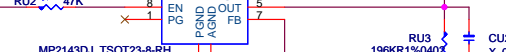
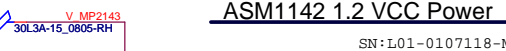
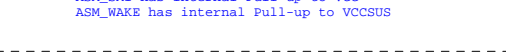
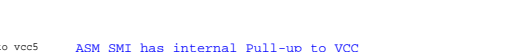
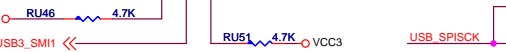
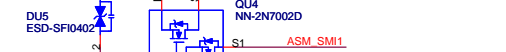
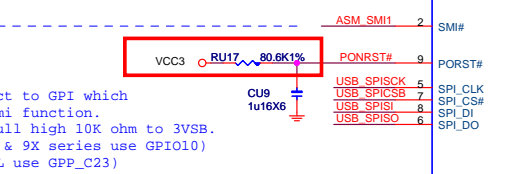
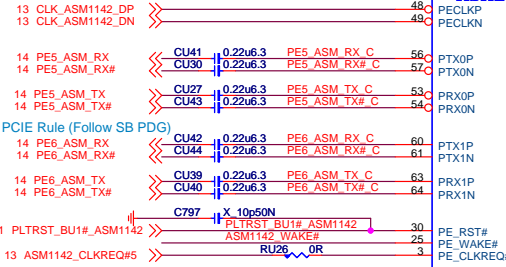
Power Consumption

	3.3V	1.2V(1.05V)	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA		1573.8(mW)
ASM2142	TDP	TDP	TDP	TDP	300mA(TDP)	TDP

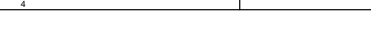
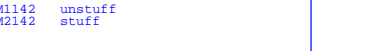
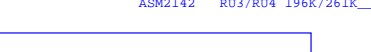
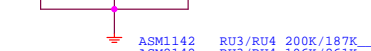
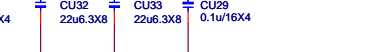
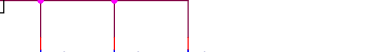
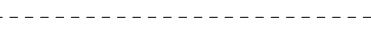
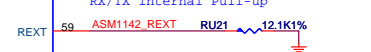
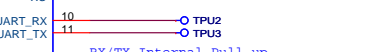
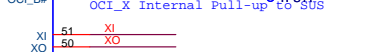
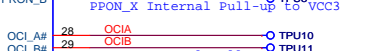
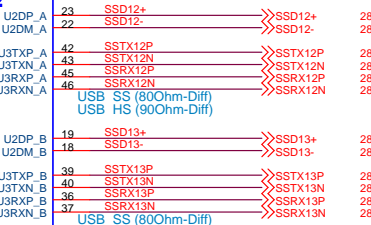
Layout Guide:

- 1.) USB3.1 to Connector Total Length < 1.5"
- 2.) VIA hole < 2

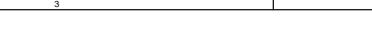
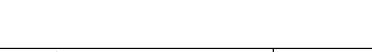
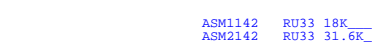
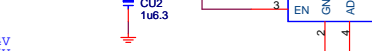
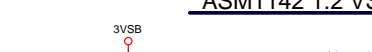
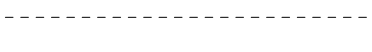
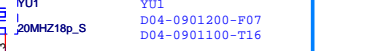
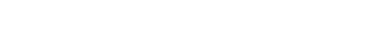
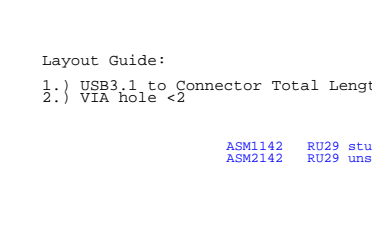
CLK Rule (Follow SB PDG)



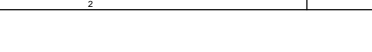
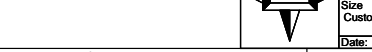
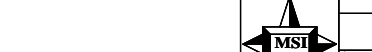
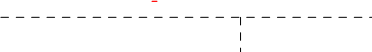
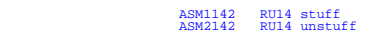
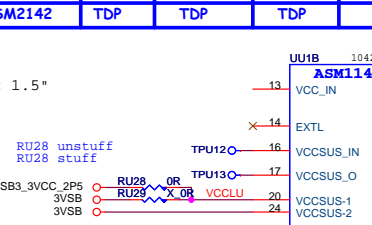
USB HS (90Ohm-Diff) Chip to Connector 1.5 inch.



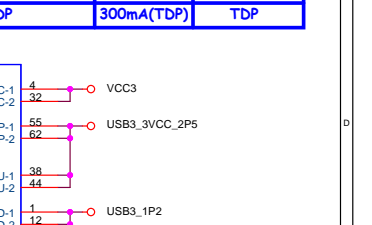
USB SS (80Ohm-Diff) Chip to Connector 1.5 inch.



USB HS (90Ohm-Diff) Chip to Connector 1.5 inch.

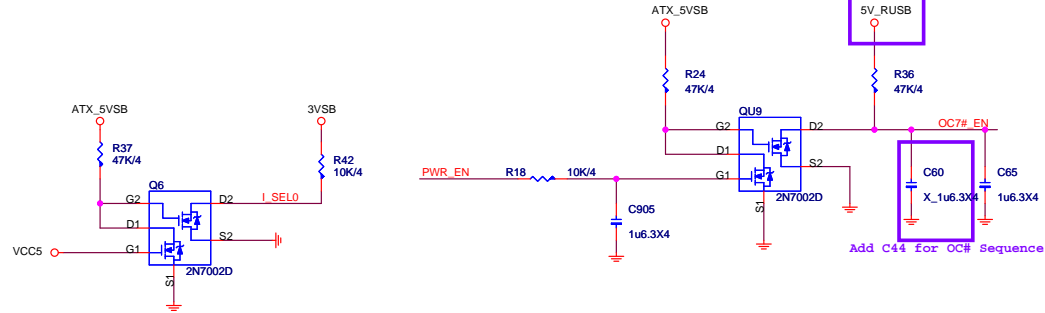


USB SS (80Ohm-Diff) Chip to Connector 1.5 inch.



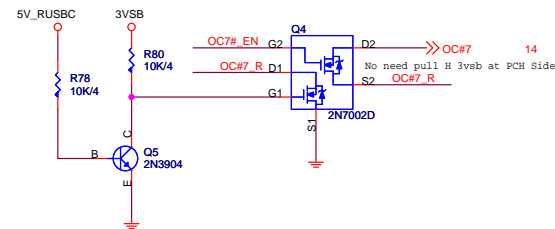
Current Mode

VBUS OC#

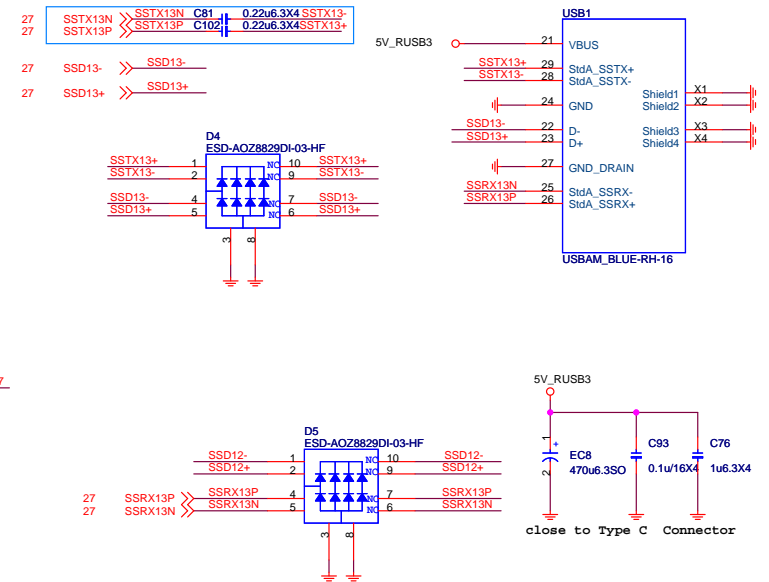


I_SELO : I_SEL1		
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

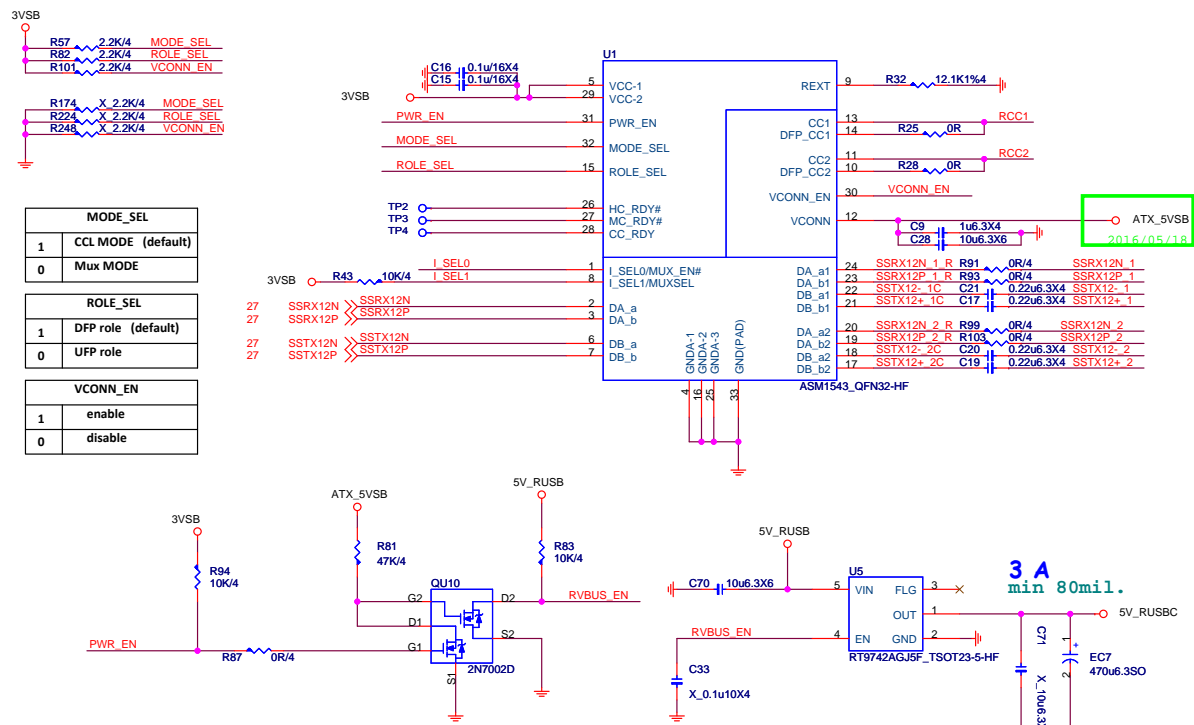
1.5A under S3 mode
3A under S0 mode



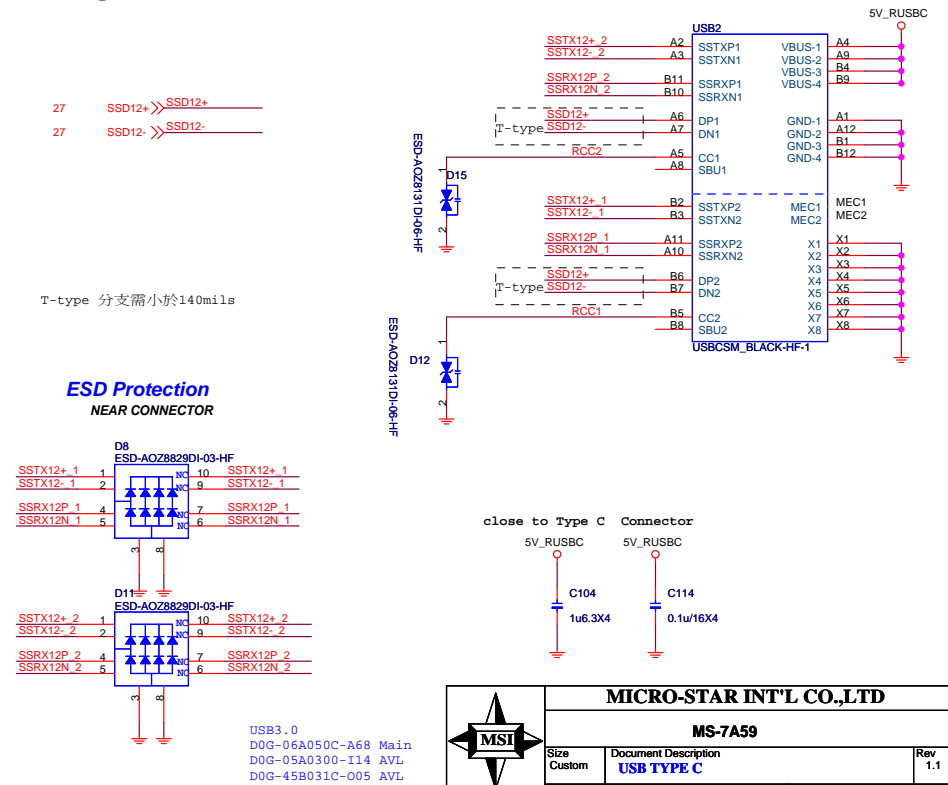
TYPE-A



USB Type-C MUX with Configuration Channel (CC)



TYPE-C

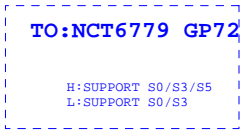


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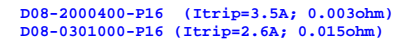
MS-7A59

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Date: Monday, September 26, 2016	Sheet 28 of 70	

USB PORT POWER



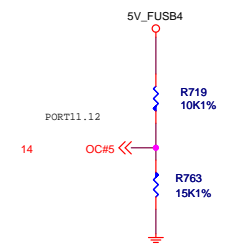
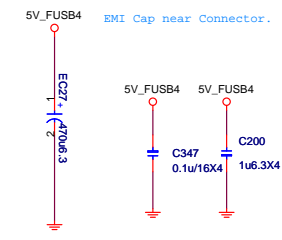
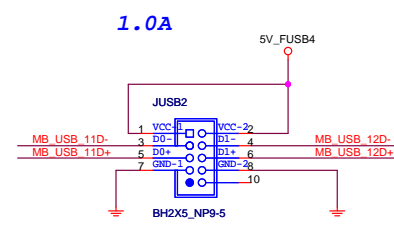
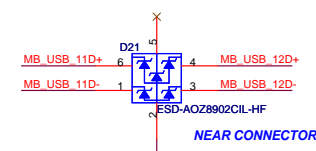
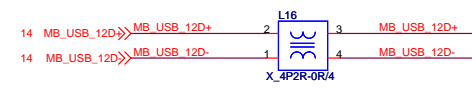
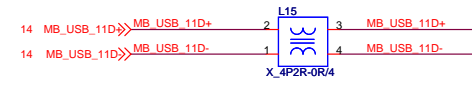
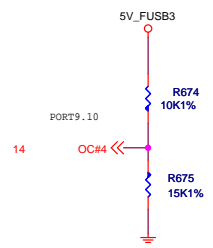
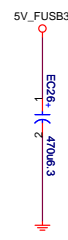
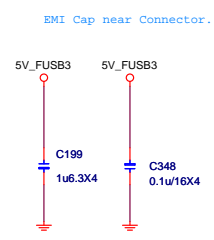
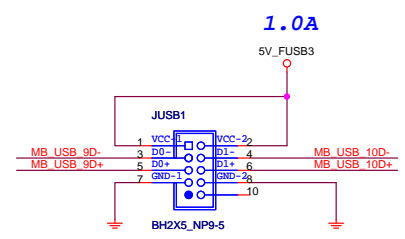
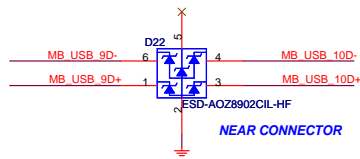
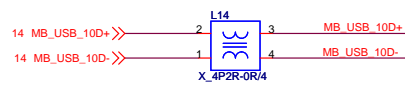
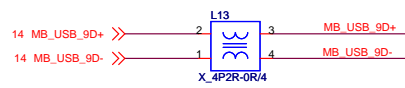
5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.



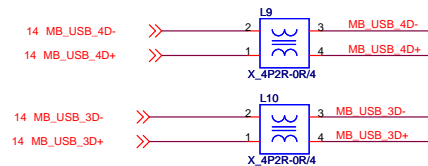
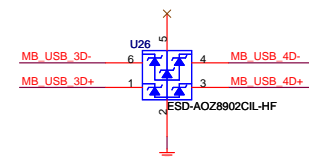
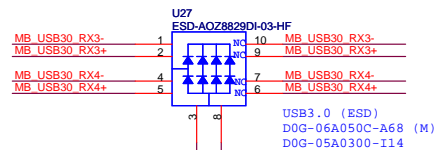
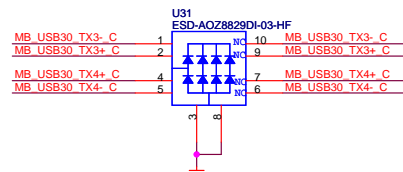
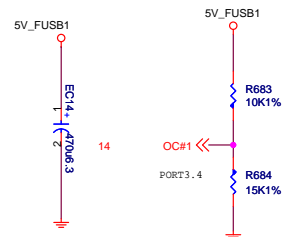
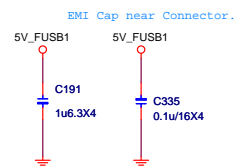
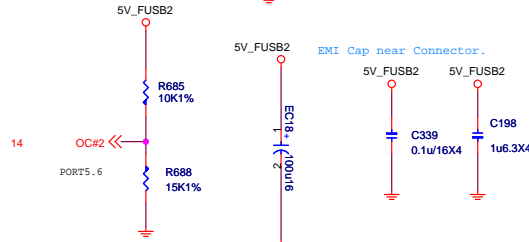
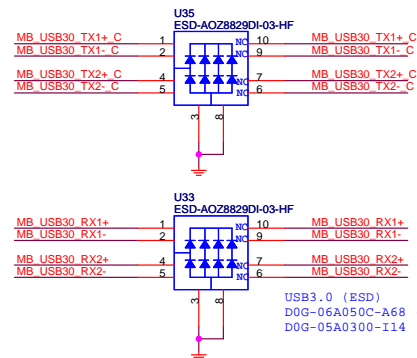
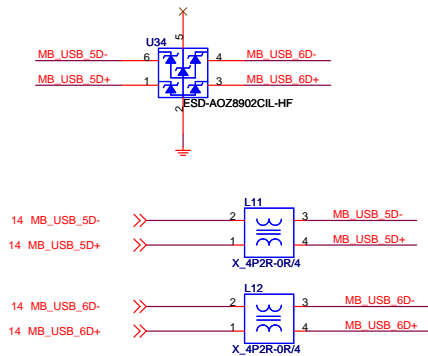
MICRO-STAR INT'L CO.,LTD

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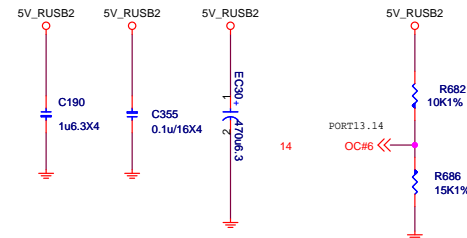
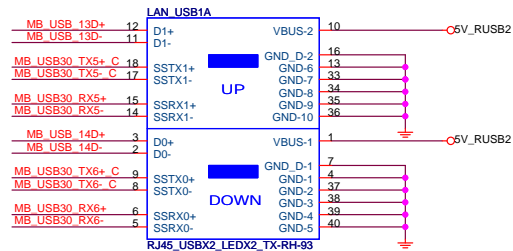
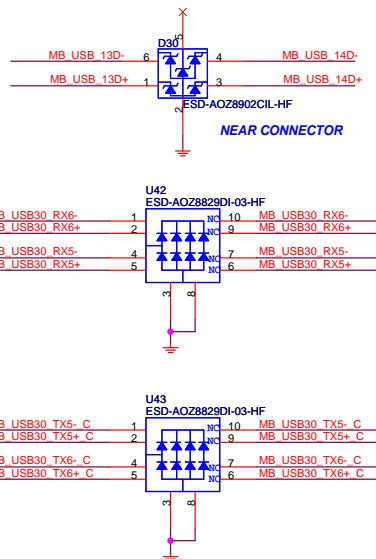
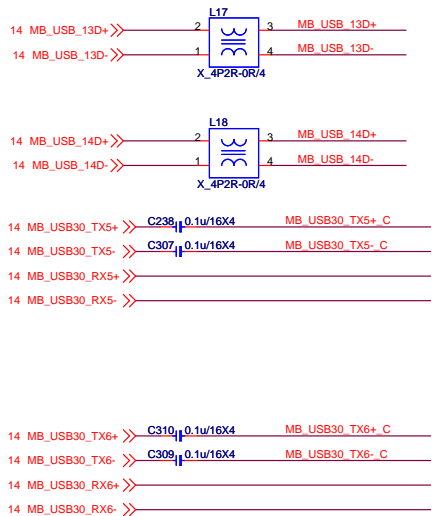


Vinafix.com

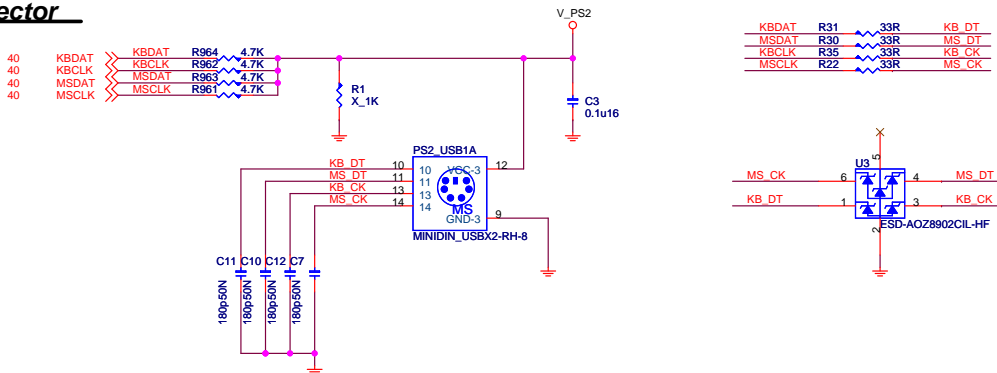


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MS-7A59			
Size Custom	Document Description Front USB30		Rev 1.1
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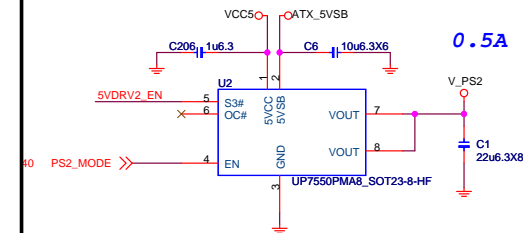
LAN USB2.0 &3.0



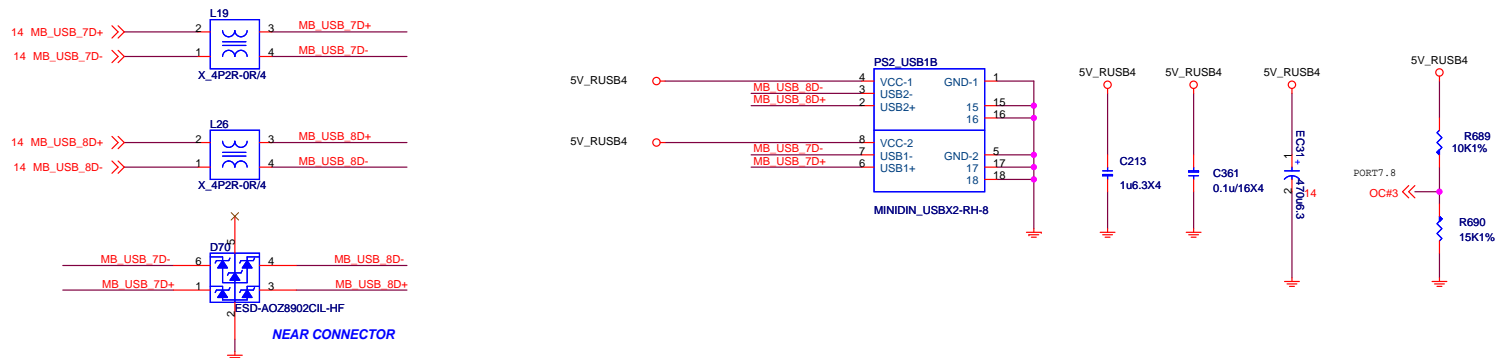
PS2 Connector



PS2 Power

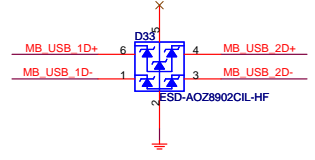
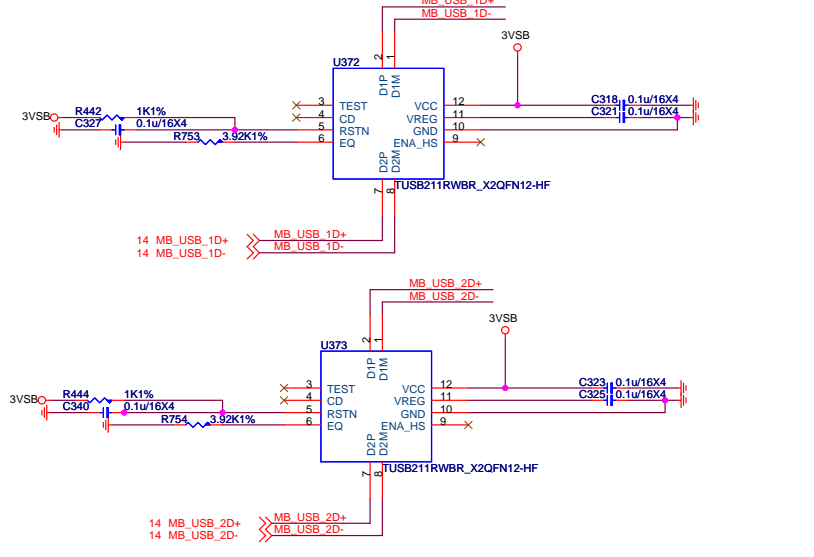
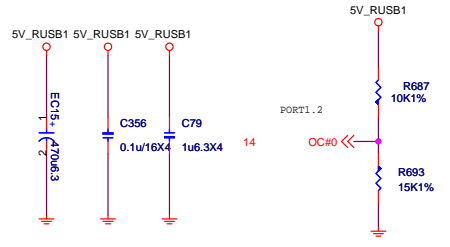
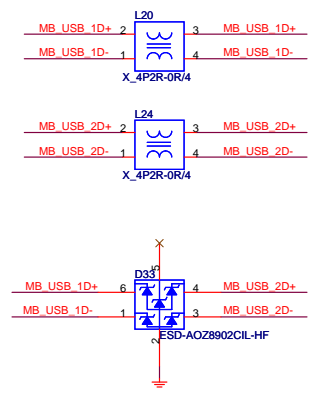
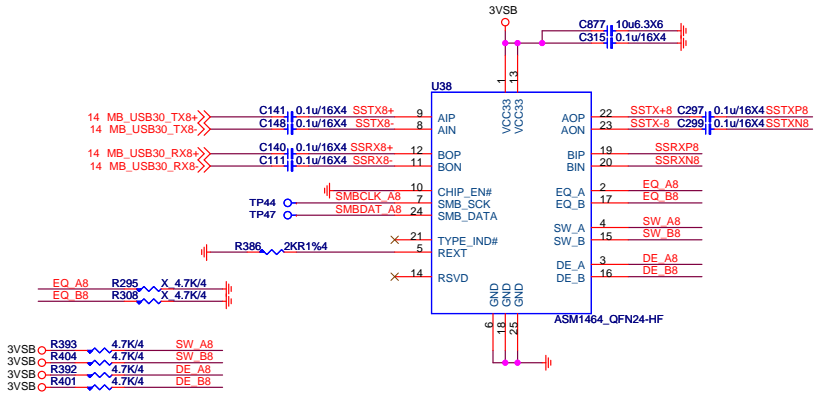
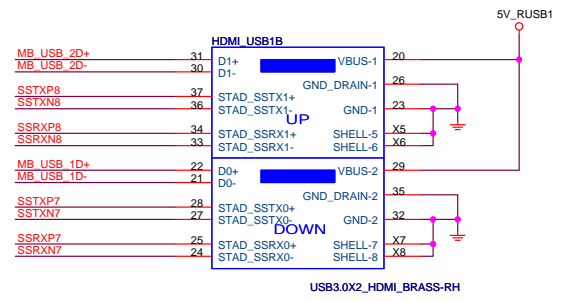
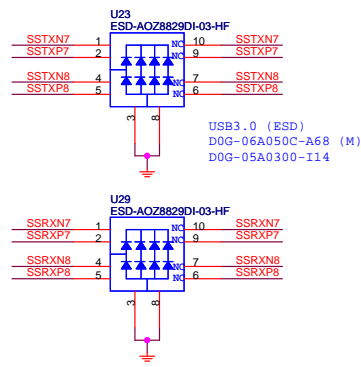
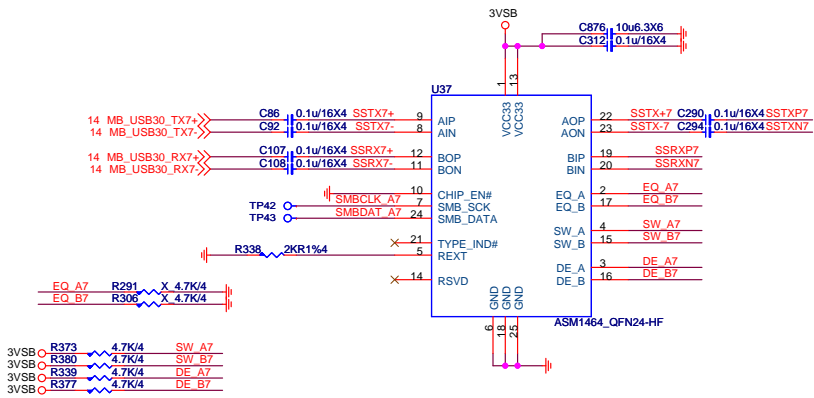


USB MODE



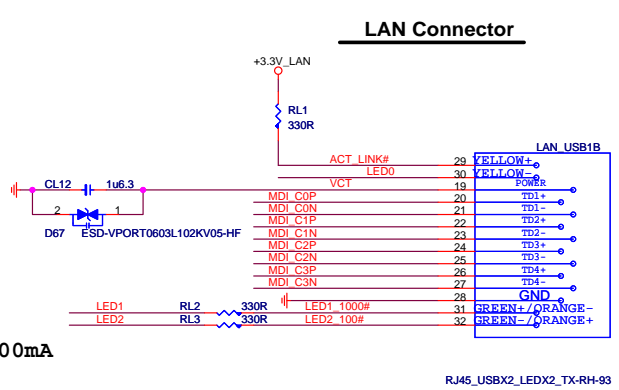
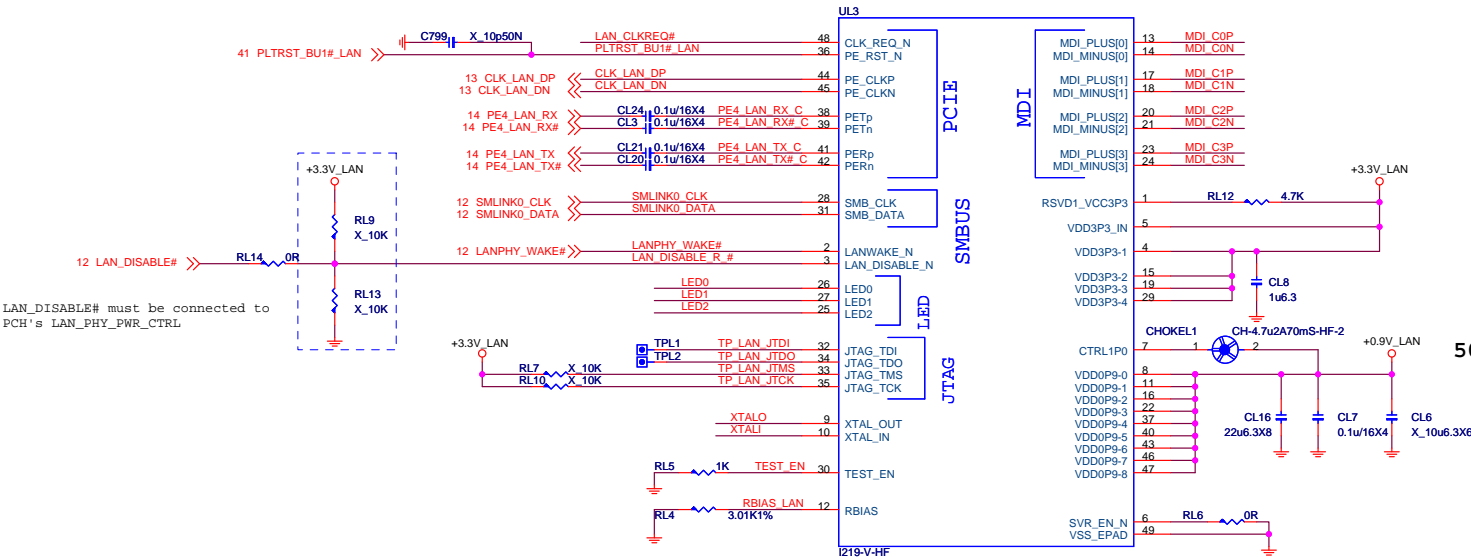
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MS-7A59		
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Custom	Real USB&PS2	1.1
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HDMI USB3.0

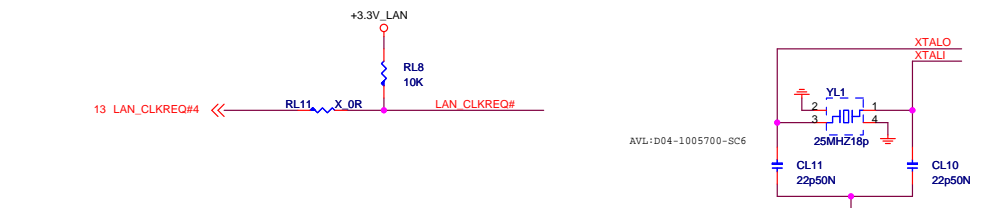


Intel Lan- i219

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

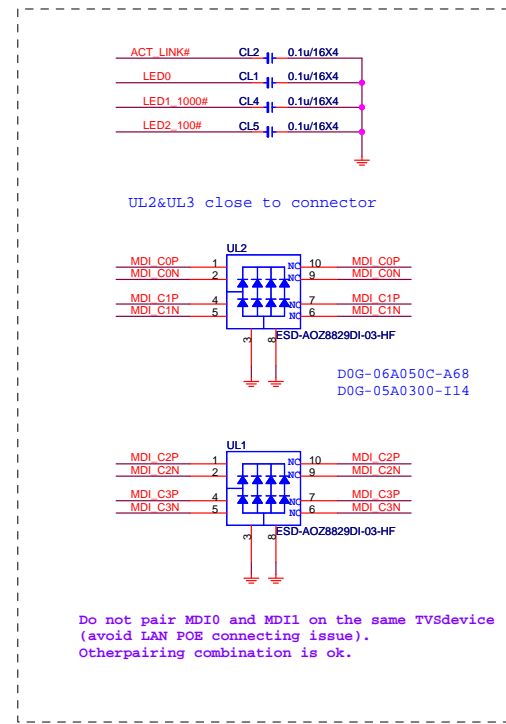
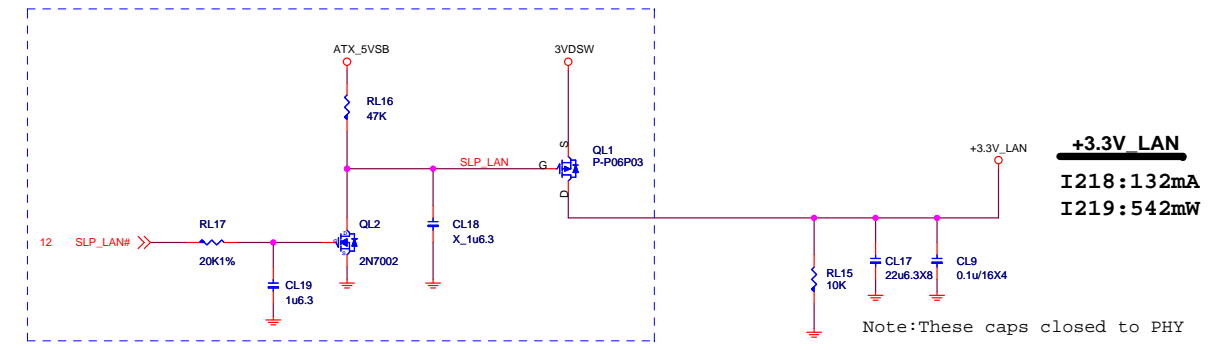


PCH's PCIECLKRQ<n> port must be mapped to PCH's PET/R<n+1>port. If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN

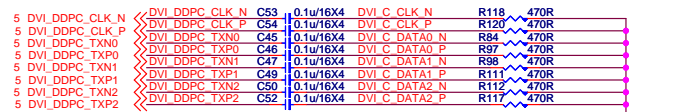


The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

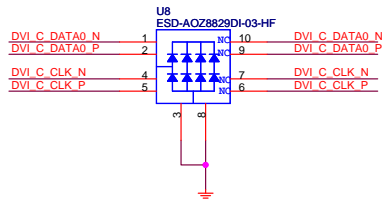
support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



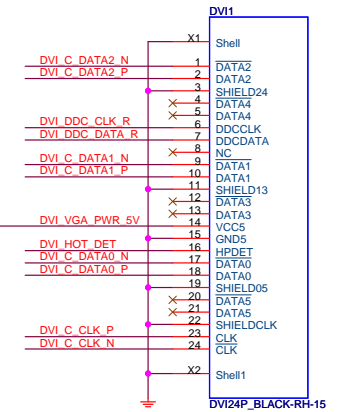
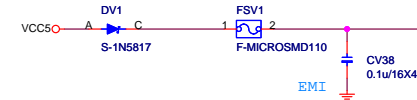
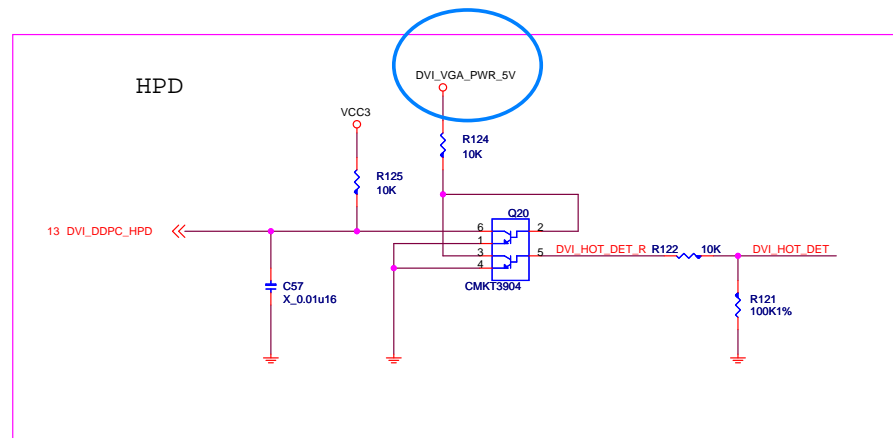
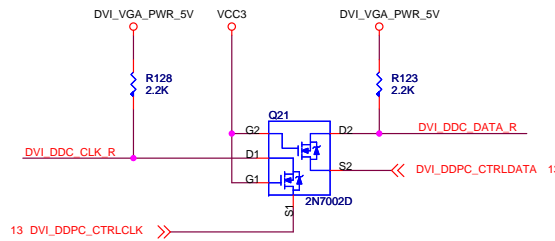
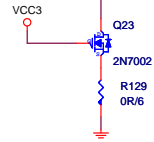
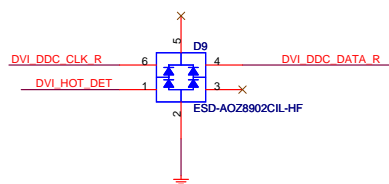
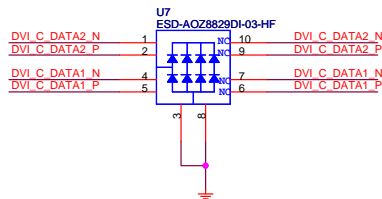
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



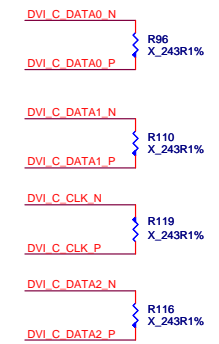
U26 AVL:D0G-05A050C-005
D0G-06A050C-A68



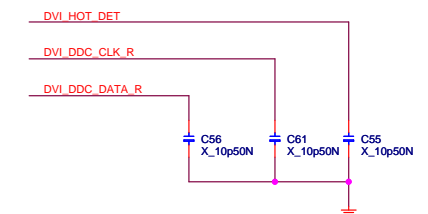
U27 AVL:D0G-05A050C-005
D0G-06A050C-A68



For EMI



EMI

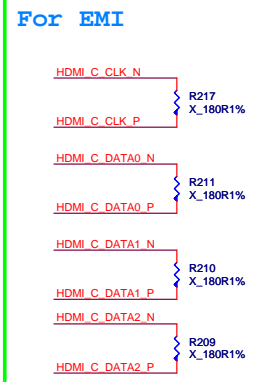
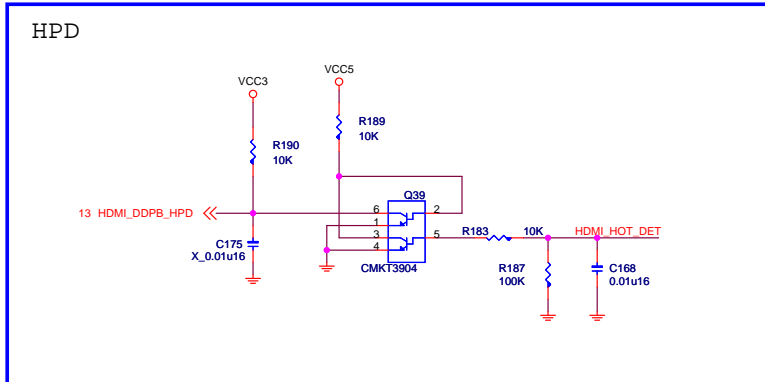
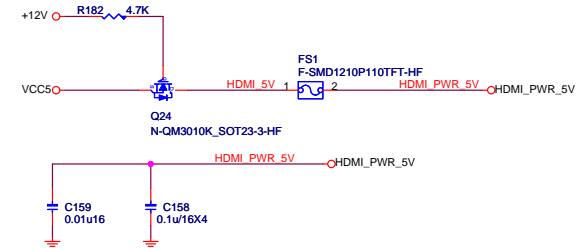
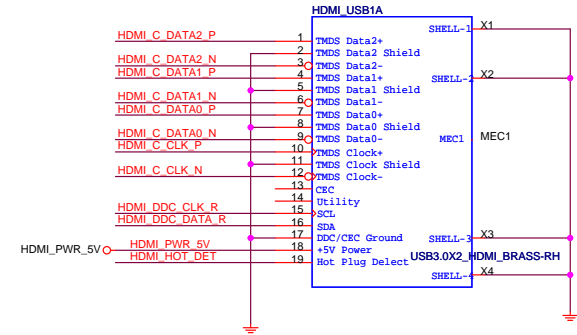
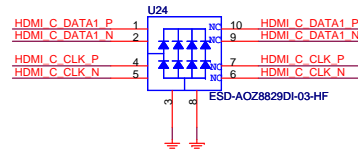
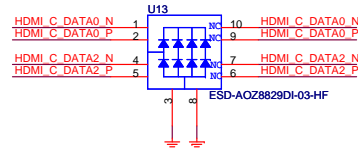
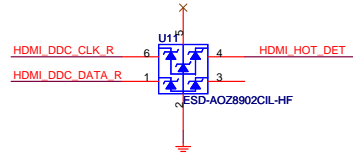
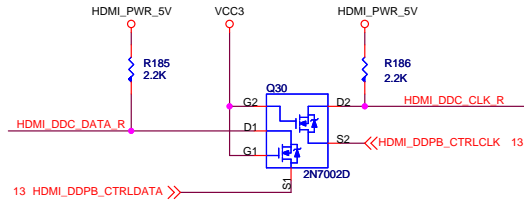
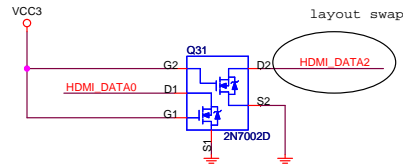
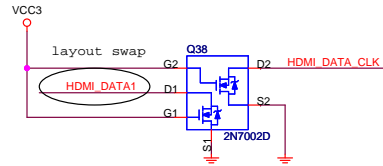
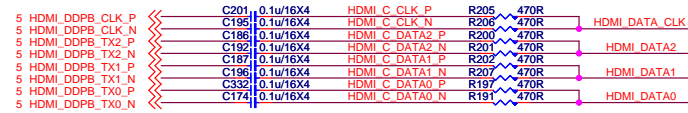


MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	DVI Connector	1.1
Date: Monday, September 26, 2016	Sheet 35 of 70	

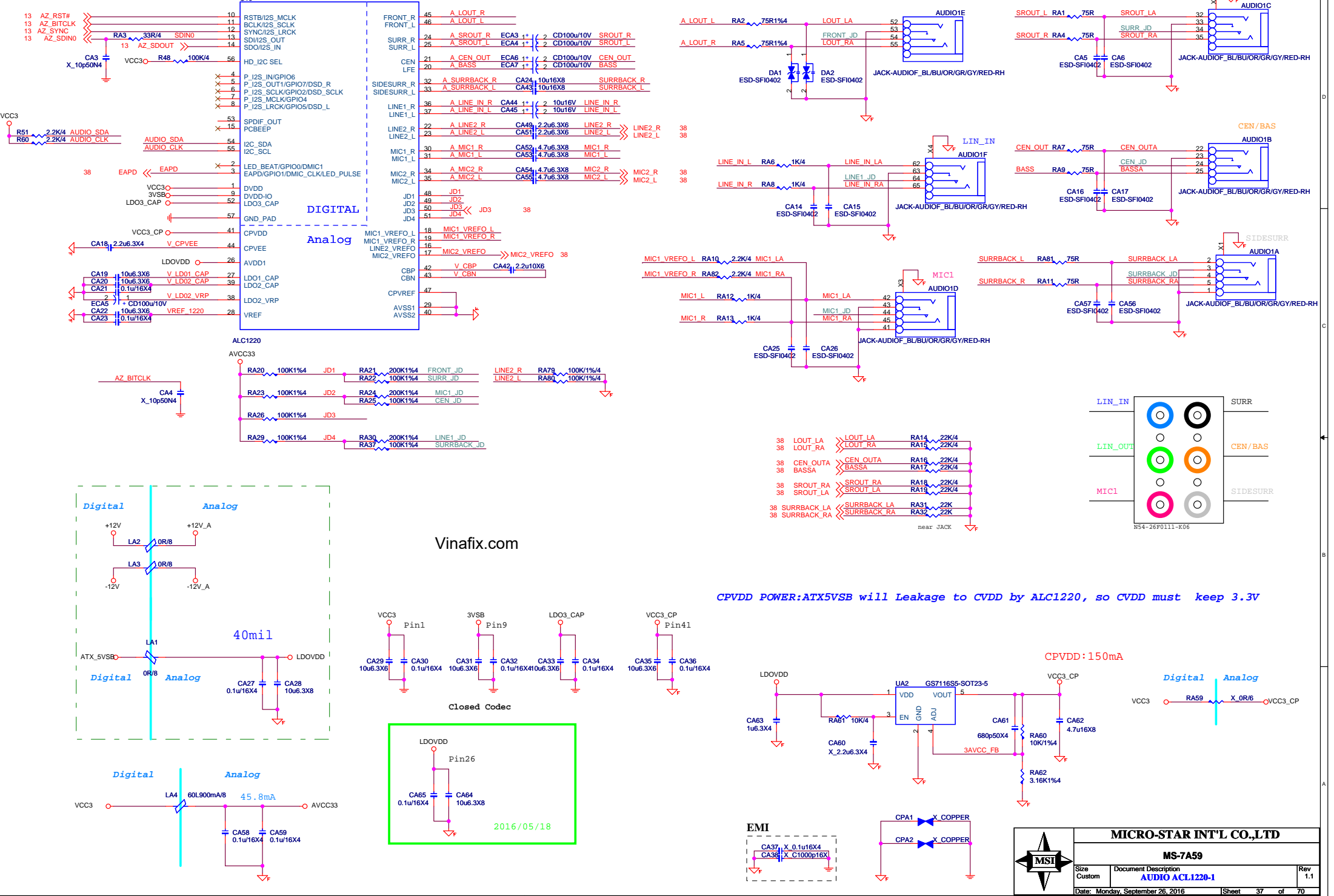
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



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MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size Custom	Document Description	Rev 1.1
Date: Monday, September 26, 2016	HDMI Connector	Sheet 36 of 70

ALC1220



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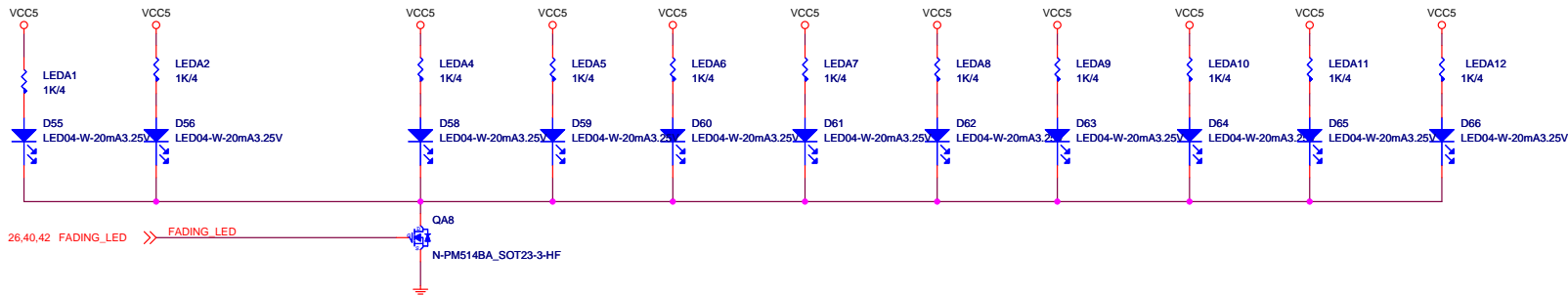
CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

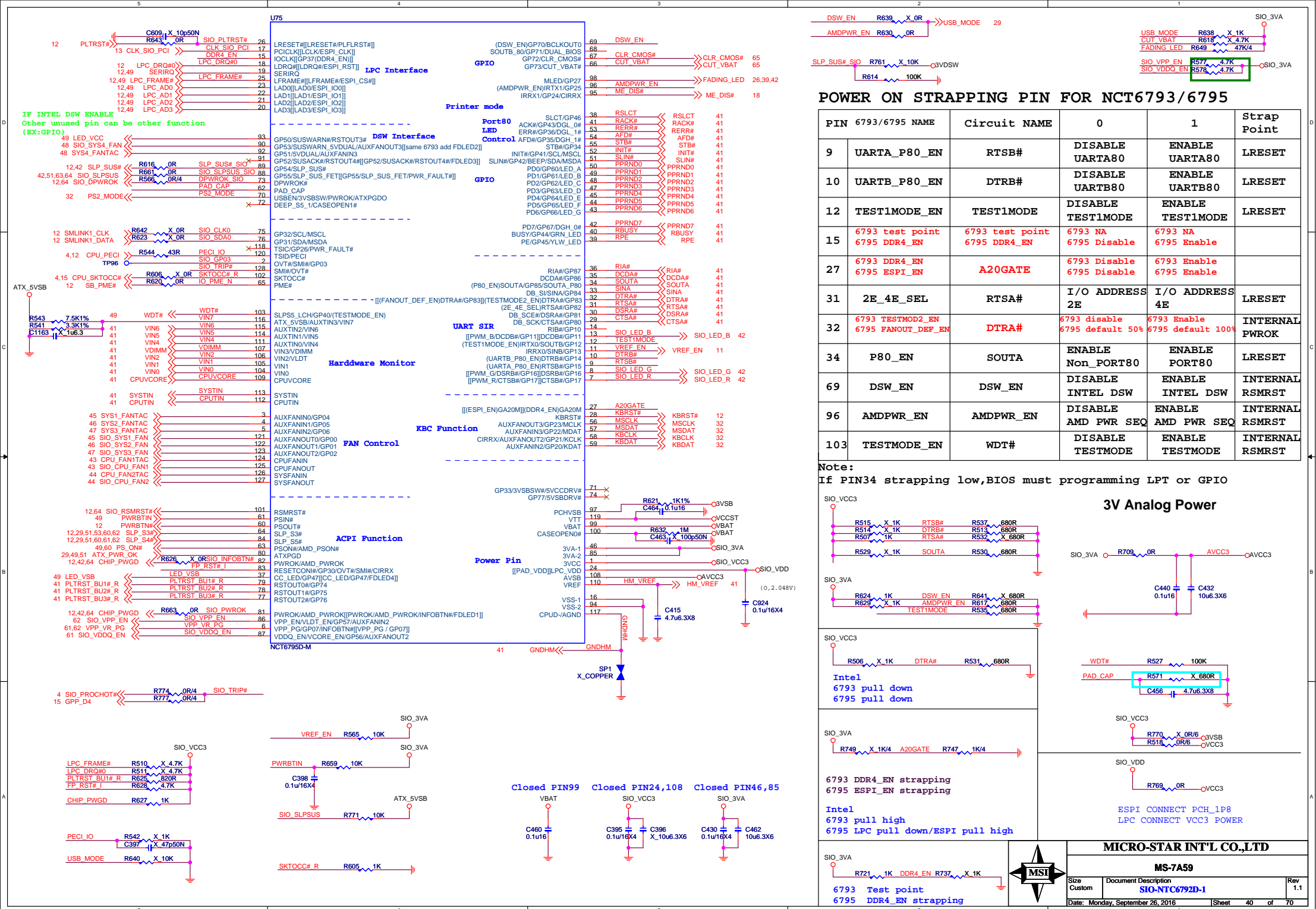
MICRO-STAR INT'L CO.,LTD

MS-7A59

Size	Document Description	Rev
Custom	AUDIO ACL1220-1	1.1
Date: Monday, September 26, 2016		Sheet 37 of 70

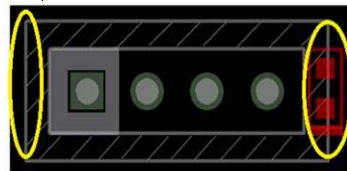
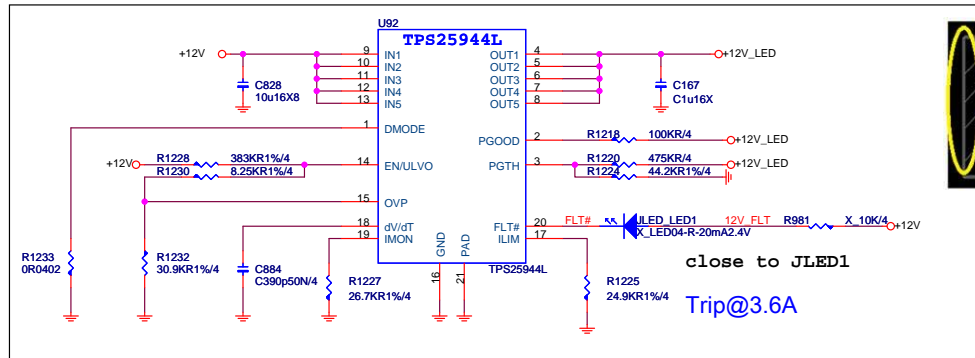
Audio moat is transparent and width 40mil



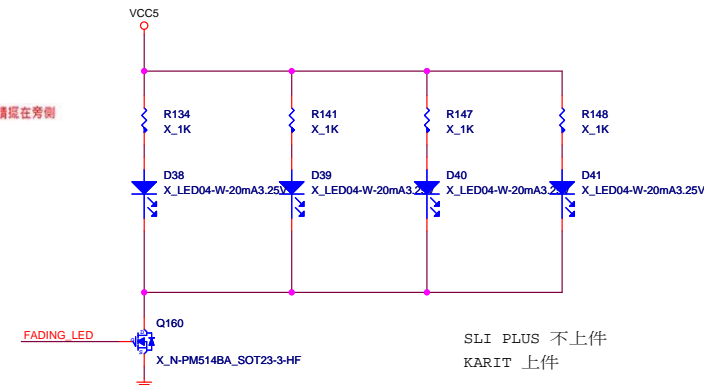


LED Control by SIO

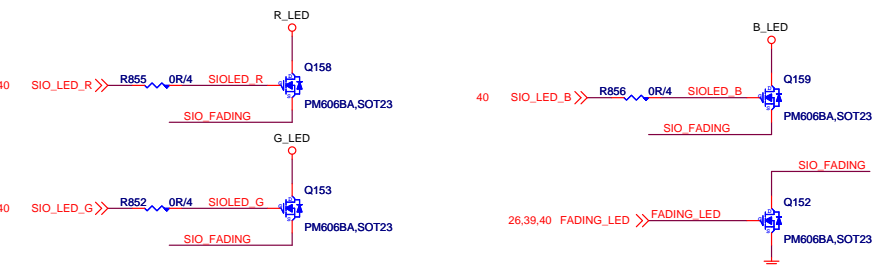
2016.07.06 Use TPS25944L



PCH LED

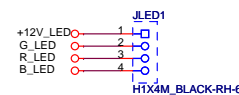
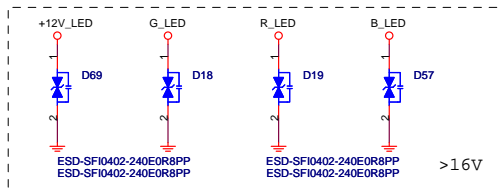
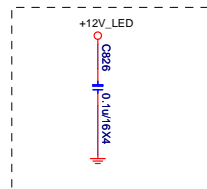


SLI PLUS 不上件
KARIT 上件

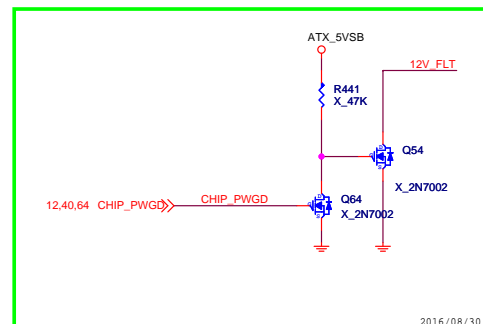
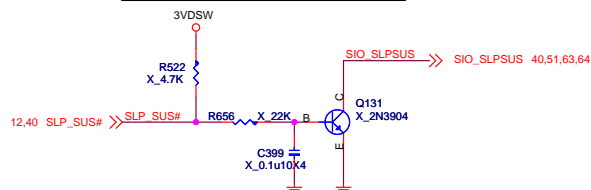


2016.08.02 Add +12V_LED 0.1uF

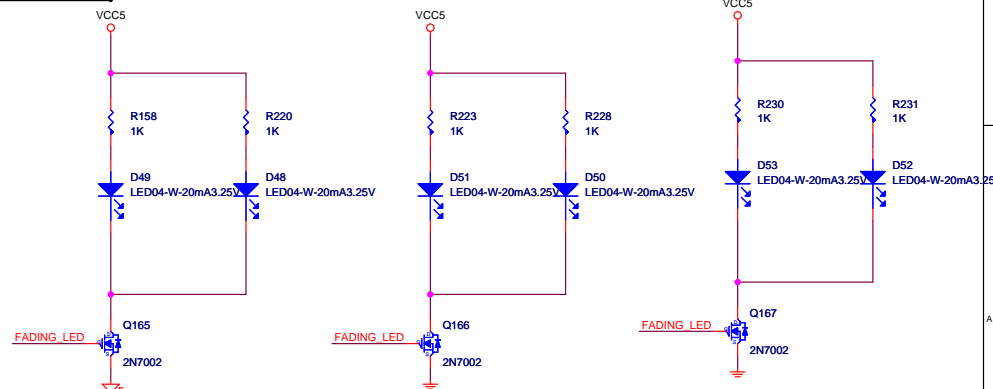
2016.08.02 stuff ESD



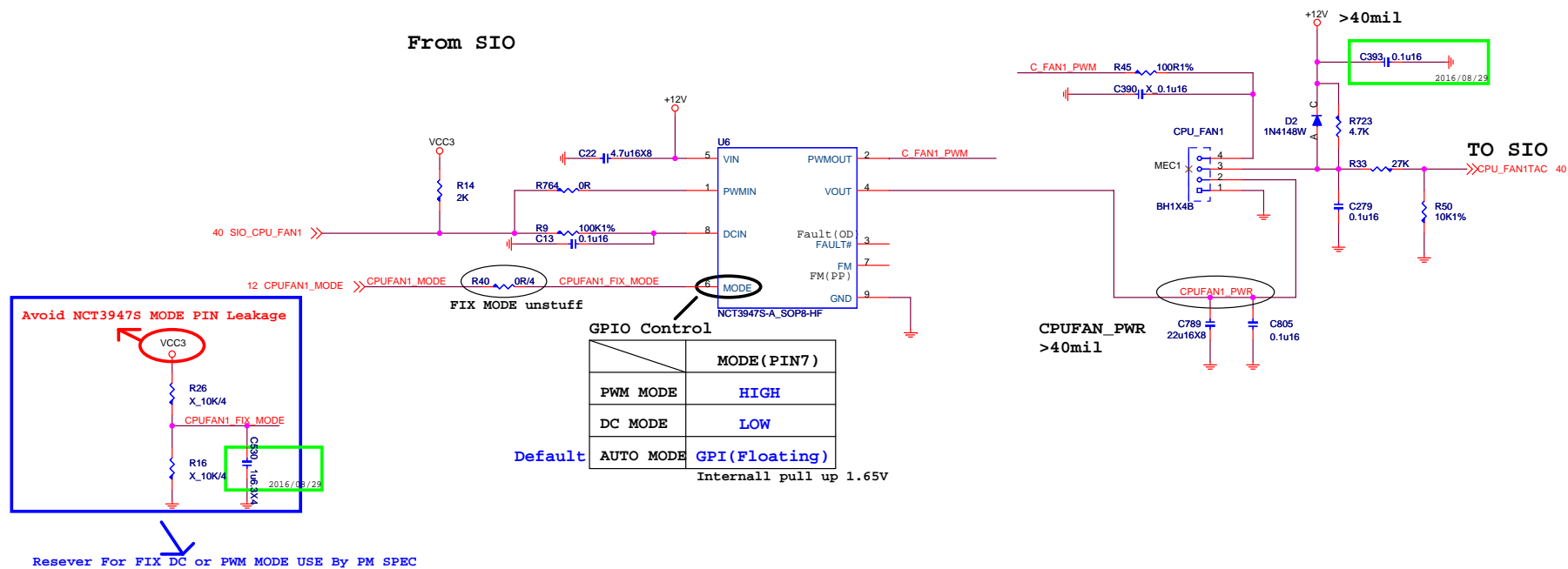
SLP_SUS Co-lay circuit



2016/08/30



MICRO-STAR INT'L CO.,LTD			
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Size	Document Description	Rev	
Custom	SIO-NTC6792D-2	1.1	
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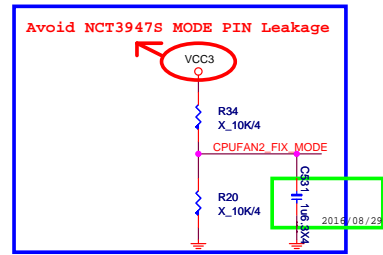
- 1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
- 2.FAULT : USE FAULT PIN Triger OVT/OC Protection,LOW Atcive (Reserve NEW IC)
- 3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)



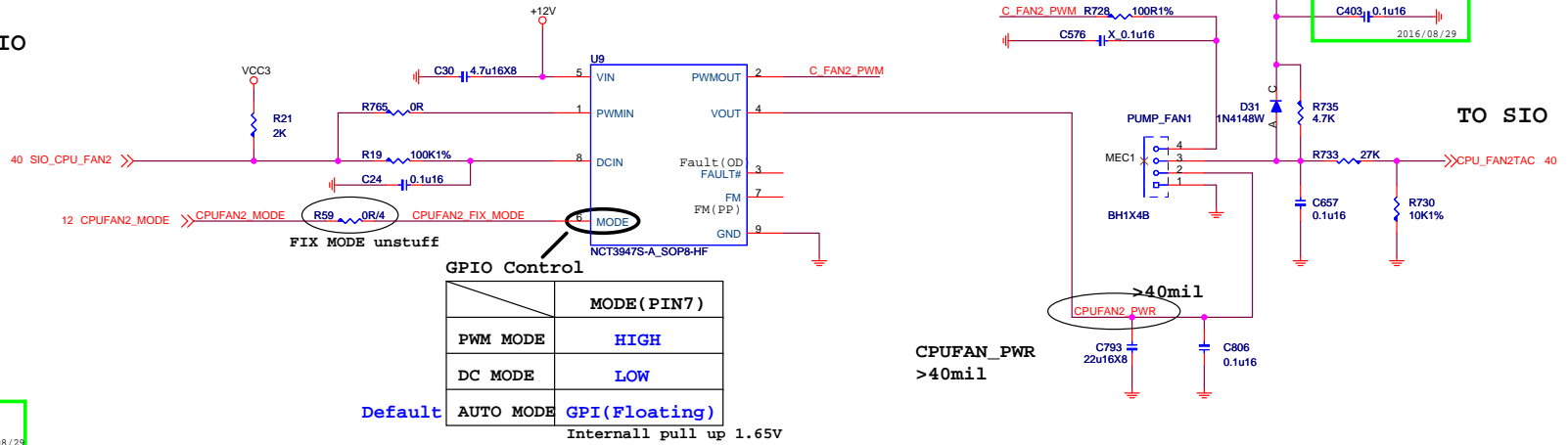
MICRO-STAR INT'L CO.,LTD		
MS-7A59		
Size Custom	Document Description CPU FAN1	Rev 1.1
Date: Monday, September 26, 2016 Sheet 43 of 70		

TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

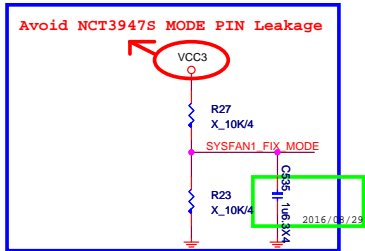
From SIO



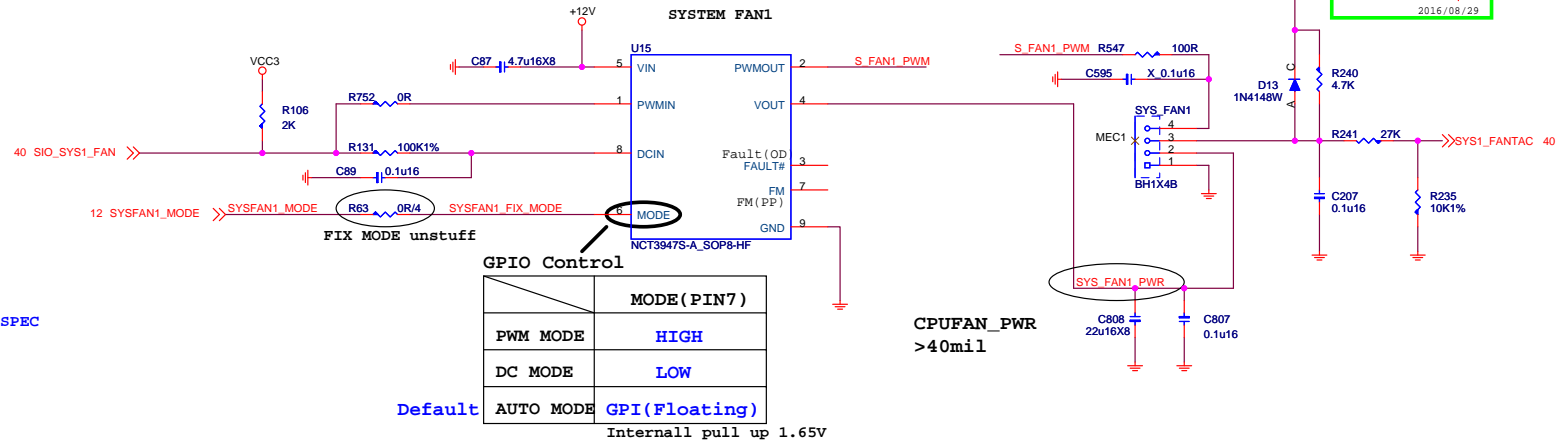
Resever For FIX DC or PWM MODE USE By PM SPEC

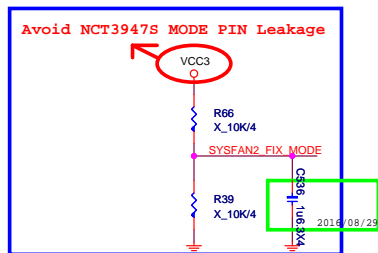


Vinafix.com

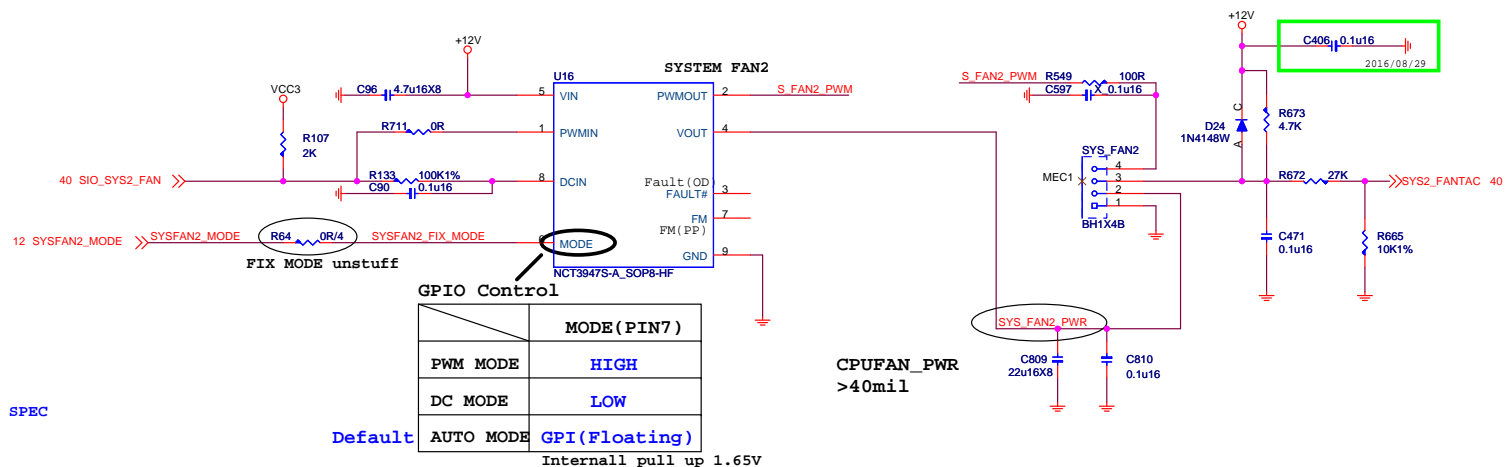


Resever For FIX DC or PWM MODE USE By PM SPEC

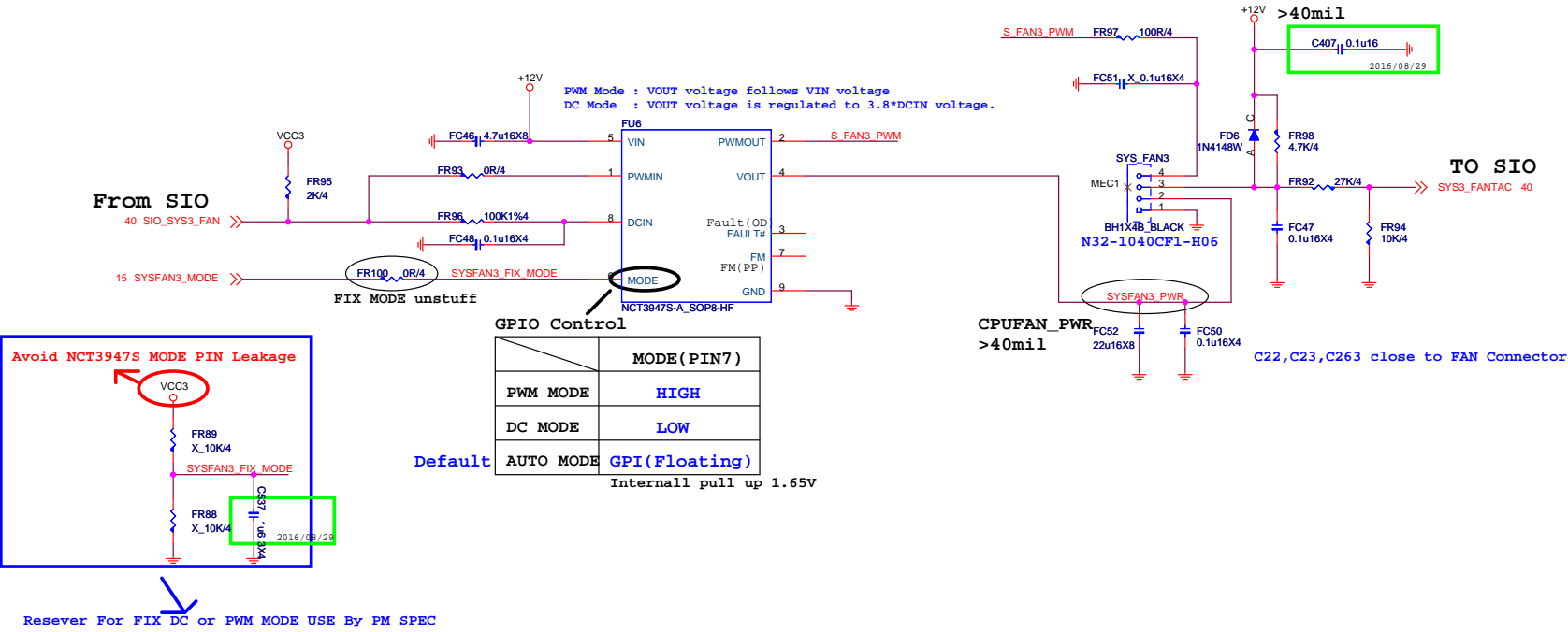




Resever For FIX DC or PWM MODE USE By PM SPEC



TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

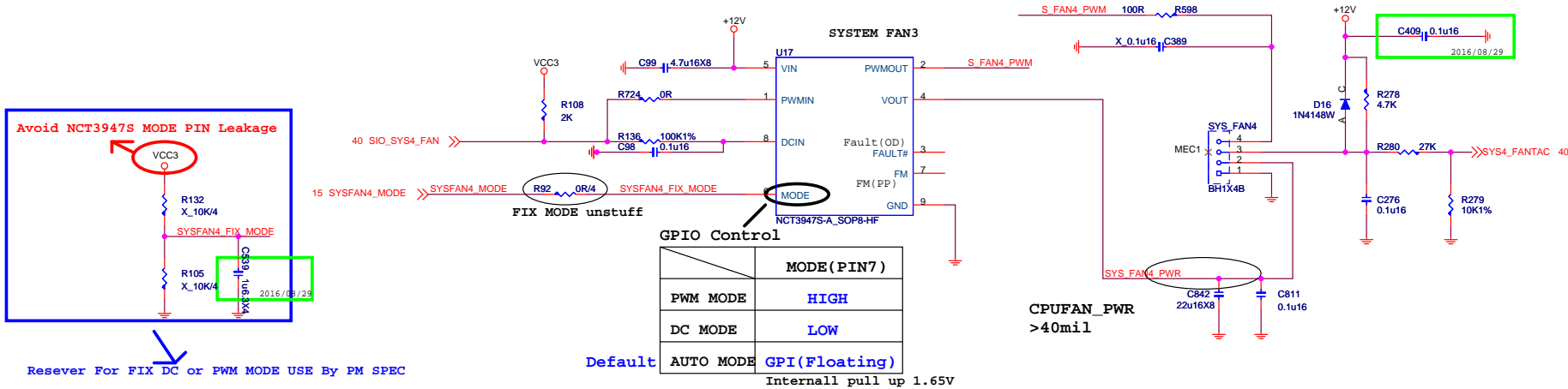


MICRO-STAR INT'L CO.,LTD

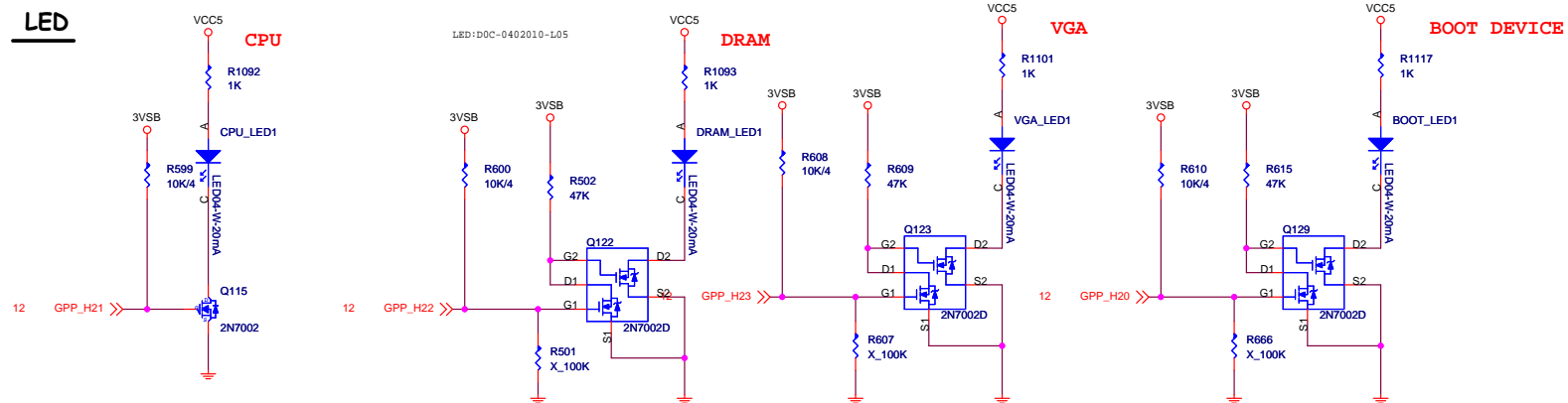
MS-7A59

Size Custom	Document Description SYSTEM FAN3	Rev 1.1
Date: Monday, September 26, 2016	Sheet 47 of 70	

TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO



LED



KRAIT GAMING LED >>WHITE:D0C-040S200-E07

開機斷電狀態下，4個LED先維持default全暗，開機通電後：

1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED減掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED減掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED減掉。
4. 因此最後正常順利開機後，三個LED燈都是減掉的。
(系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作)

LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

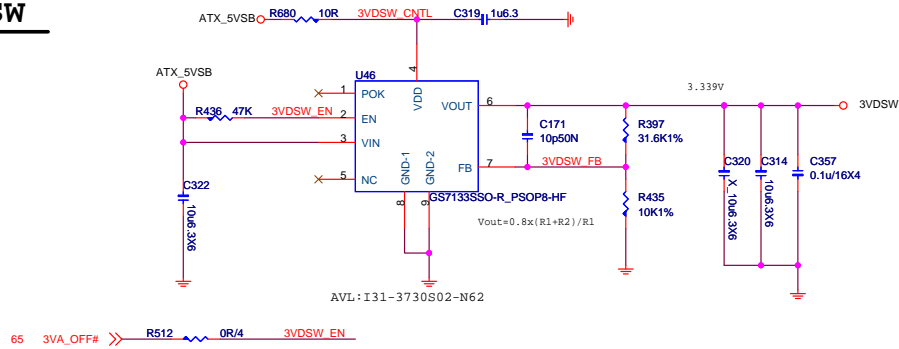


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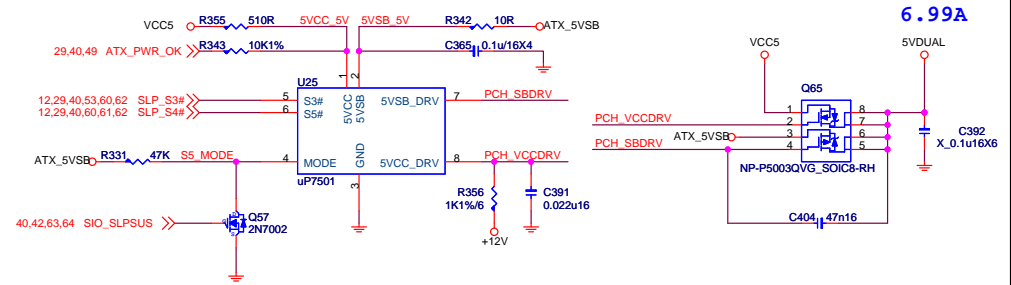
Size Custom	Document Description ATX Power/F_Panel	Rev 1.1
Date: Monday, September 26, 2016	Sheet 50 of 70	

3VDSW



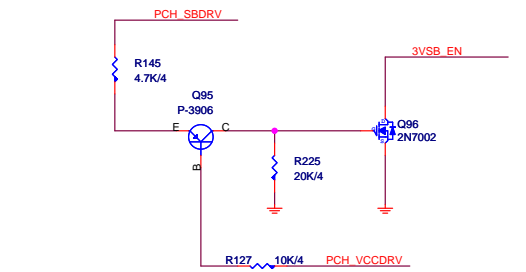
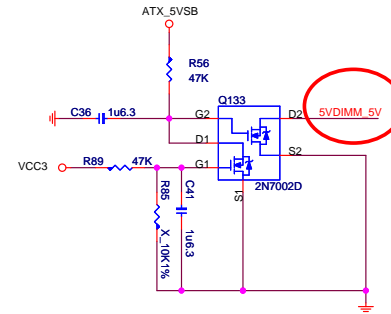
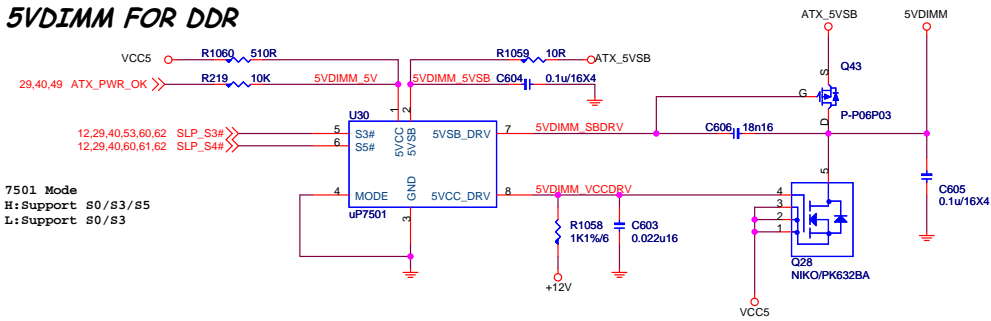
5VDUAL

5VDUAL is power source of 1P0SB



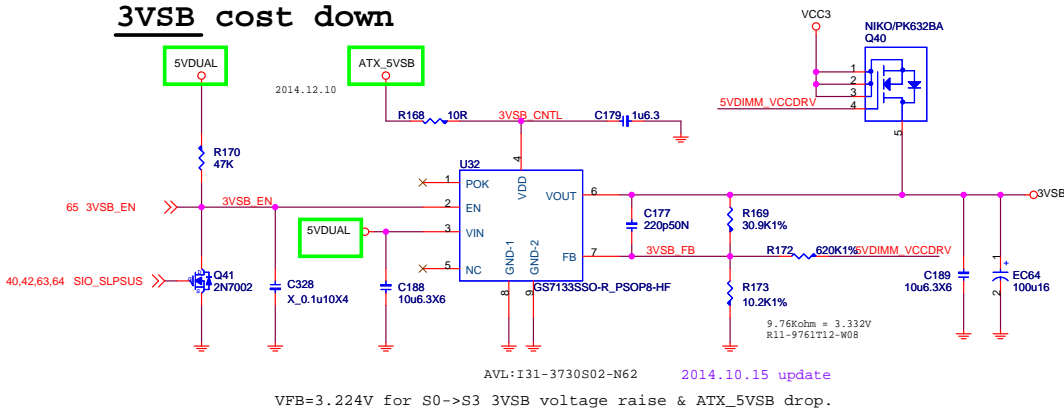
6.99A

5VDIMM FOR DDR



防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有droop

3VSB cost down

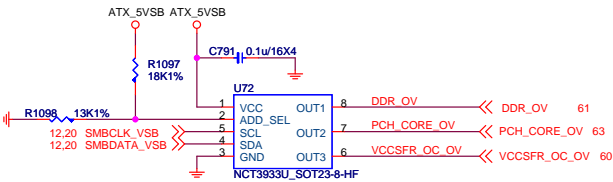


VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.

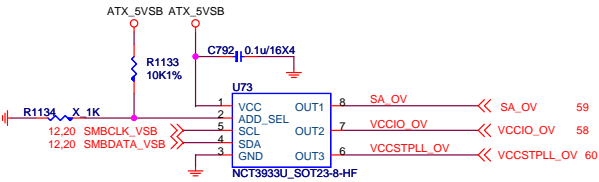
MICRO-STAR INT'L CO.,LTD			
MS-7A59			
Size	Document Description	Rev	
Custom	ACPI UP	1.1	
Date:	Monday, September 26, 2016	Sheet	51 of 70

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



0x20:RH=10K,RL=OPEN



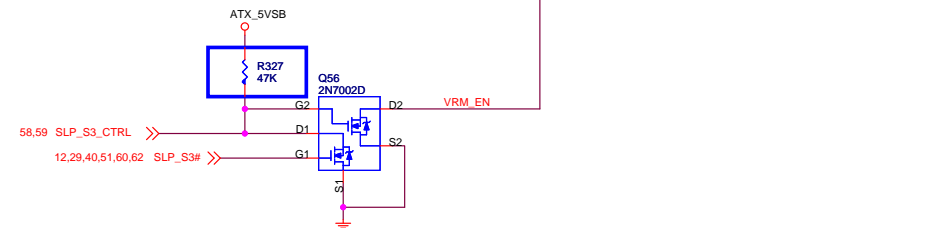
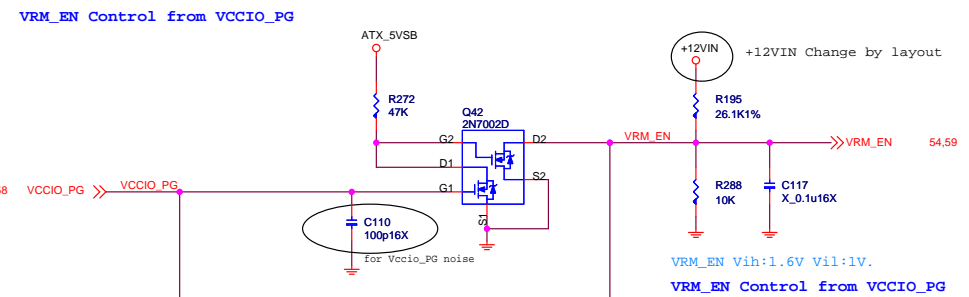
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



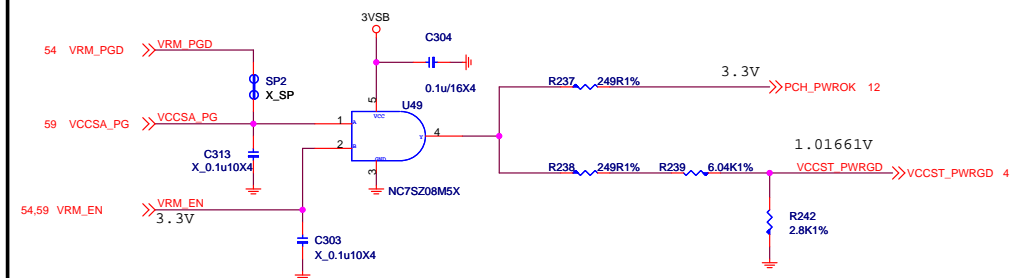
MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description OV-NCT3933/GPIO-NCT5605	Rev 1.1
Date: Monday, September 26, 2016	Sheet 52 of 70	



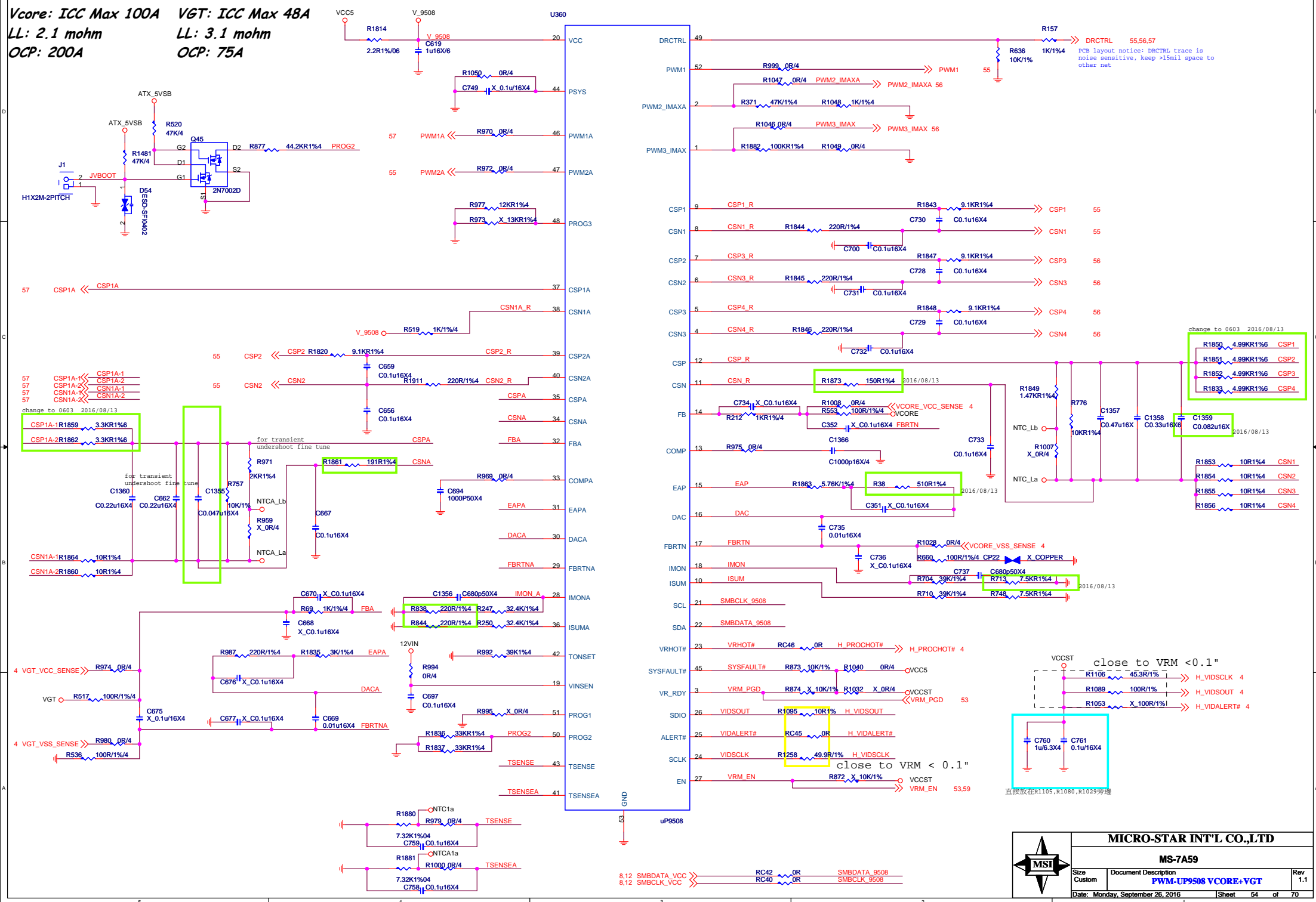
```
VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC,pull up VCCSA
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.
```



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Size Custom	Document Description Rear I/O PS2	Rev 1.1
Date: Monday, September 26, 2016		Sheet 53 of 70

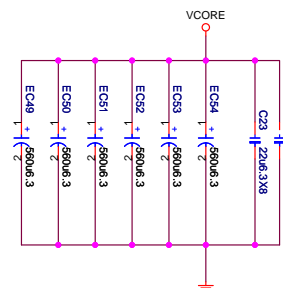
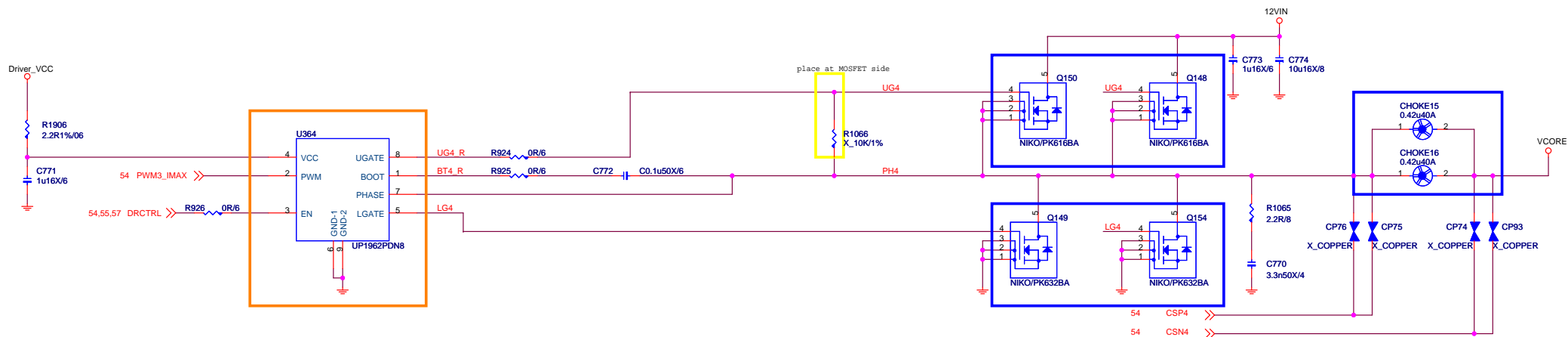
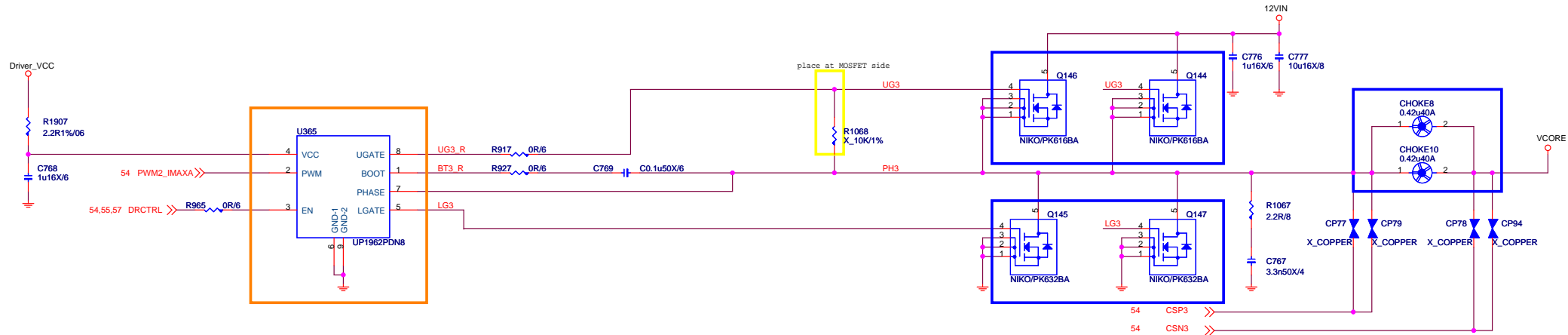
Vcore: ICC Max 100A	VGT: ICC Max 48A
LL: 2.1 mohm	LL: 3.1 mohm
OCP: 200A	OCP: 75A



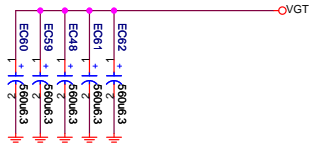
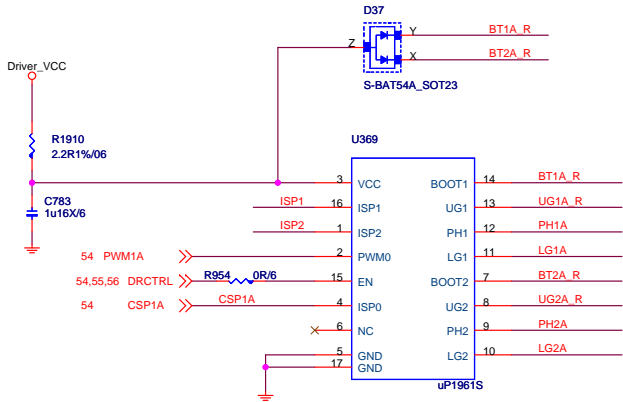
MICRO-STAR INT'L CO.,LTD

MS-7A59

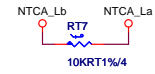
Size Custom	Document Description PWM-UP9508 VCORE+VGT	Rev 1.1
Date: Monday, September 26, 2016		Sheet 54 of 70



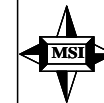
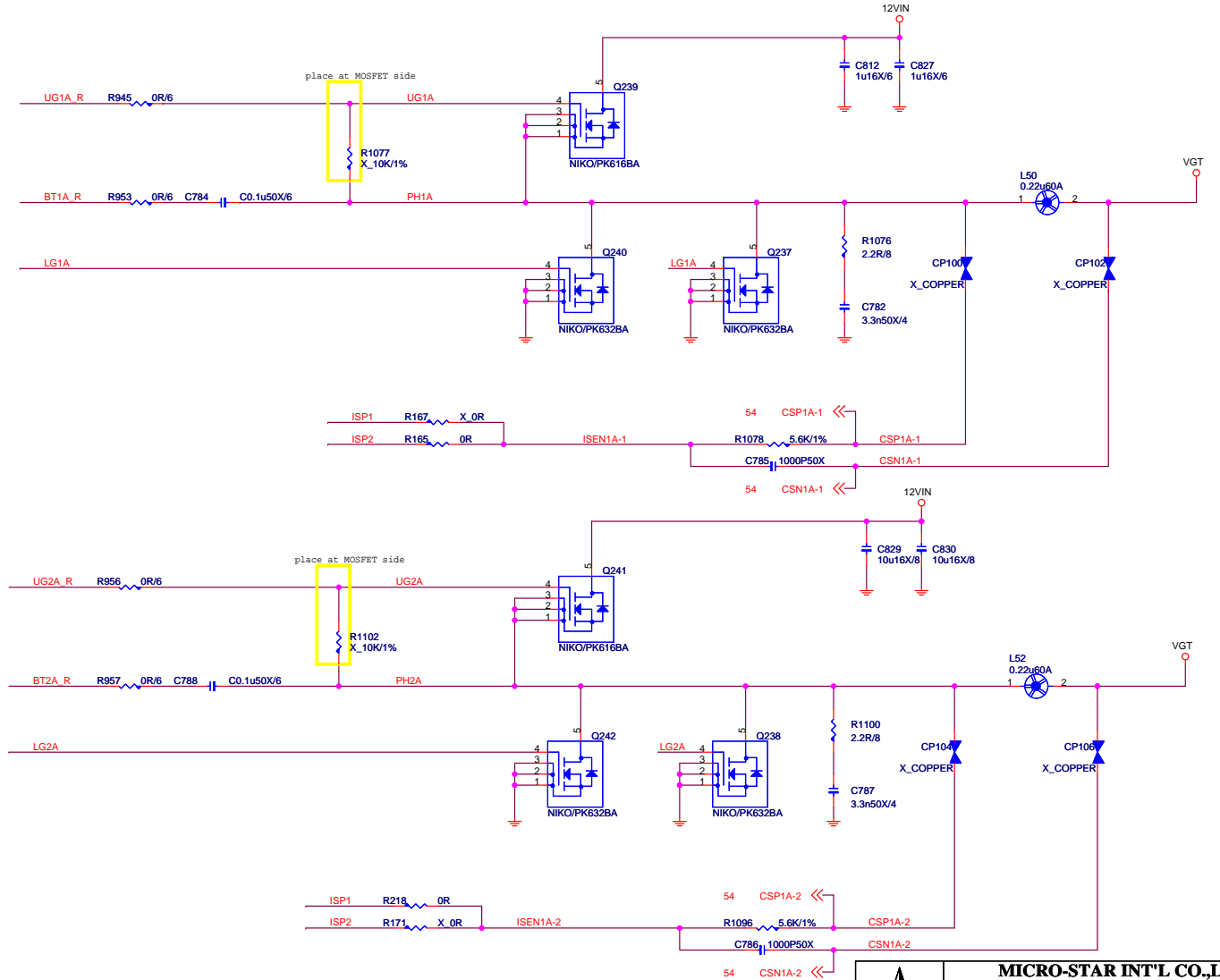
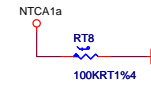
Vinafix.com



RT7 放在L50與L52中間



RT8放置在VccGT 這組switching power 最熱的地方



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	VGT MOS-PHASE 1~2	1.1
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VCCIO

0.95V; 5.5A

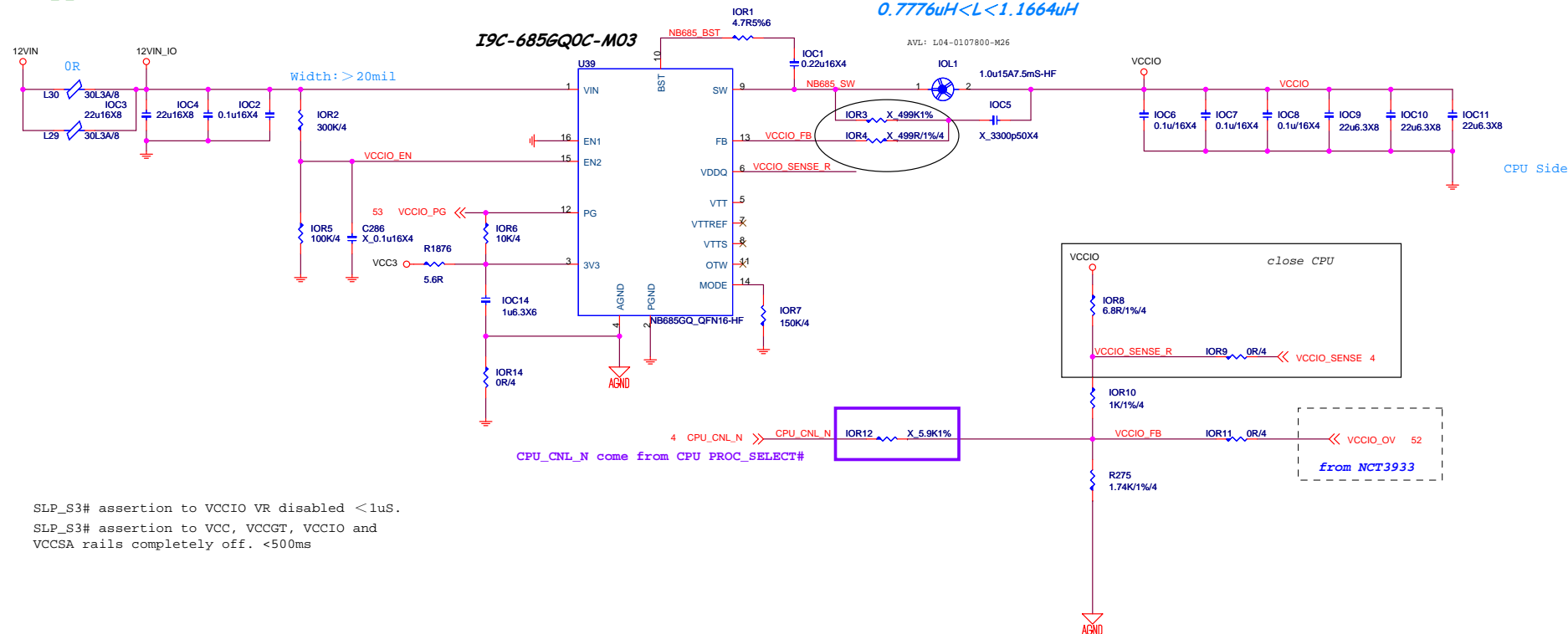
support OV=>NB685

IMAX 10A

ILIMIT=10A~12A

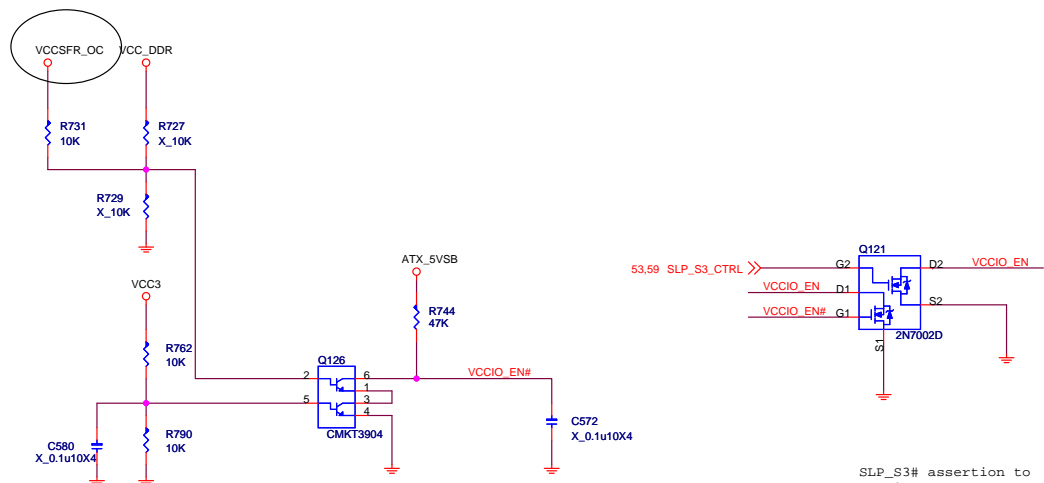
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0.7776uH<L<1.1664uH



SLP_S3# assertion to VCCIO VR disabled <1uS.

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms



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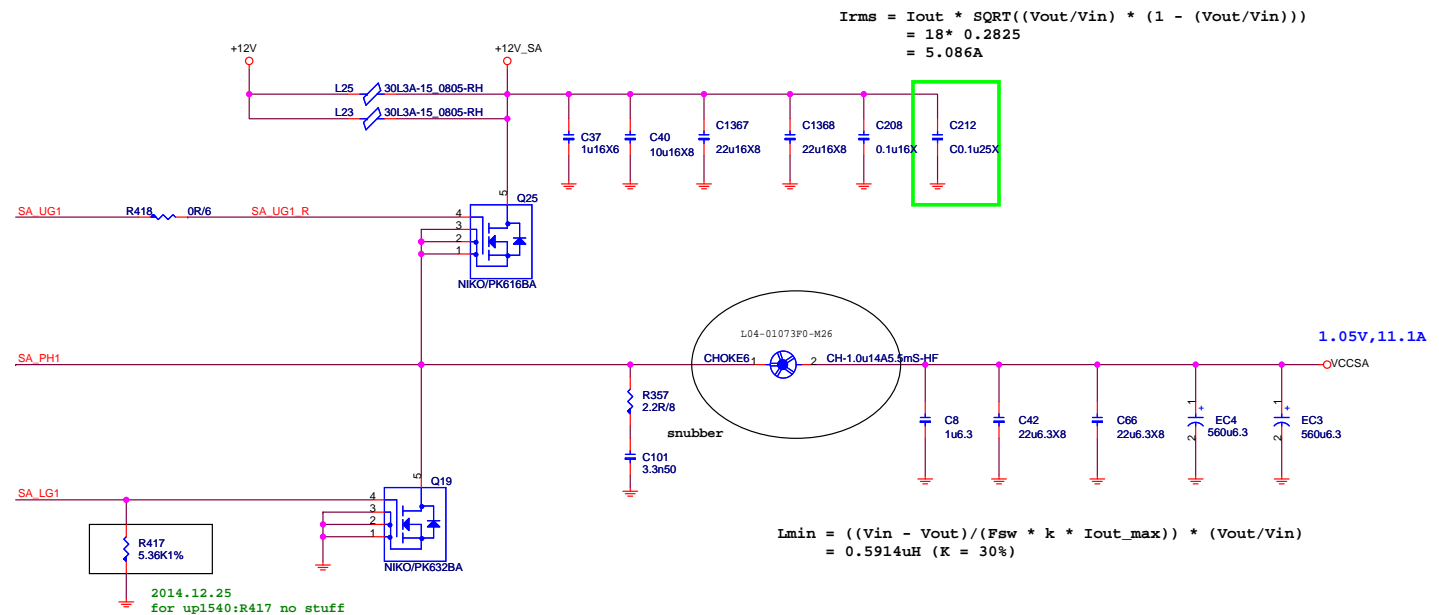
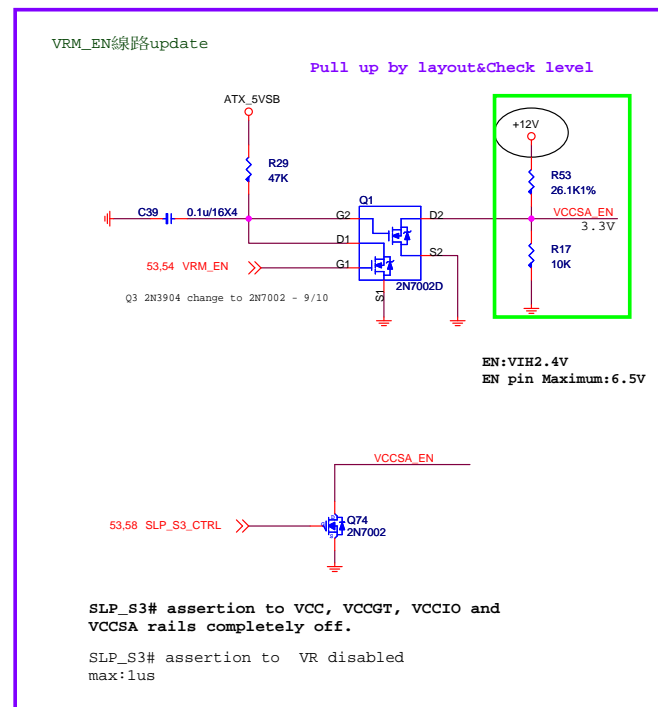
MS-7A59

Size	Document Description	Rev
Custom	CPU PWR_VCCIO	1.1
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```

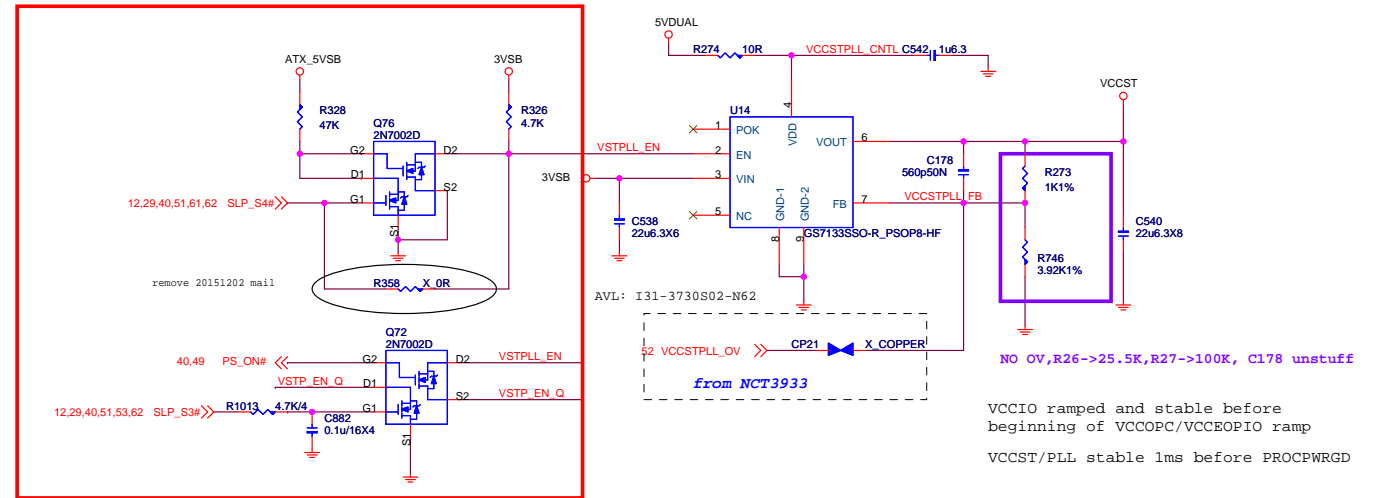
-----
Rdson(10V)10V
D03-4C05N03-005 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

```

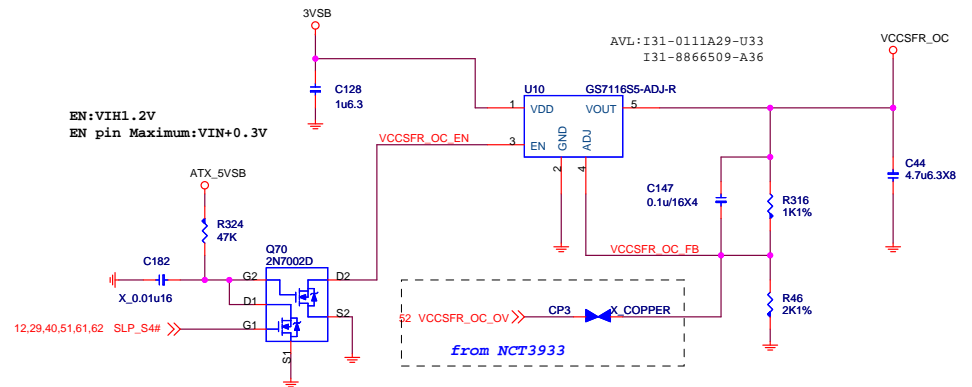


For Cost down VCCST&VCCPLL merge

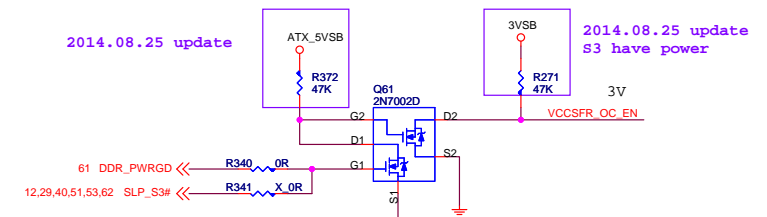
for Gaming3/5, Classic, ECO
and H110



2014.08.21 update



2014.08.25 update



MICRO-STAR INT'L CO.,LTD

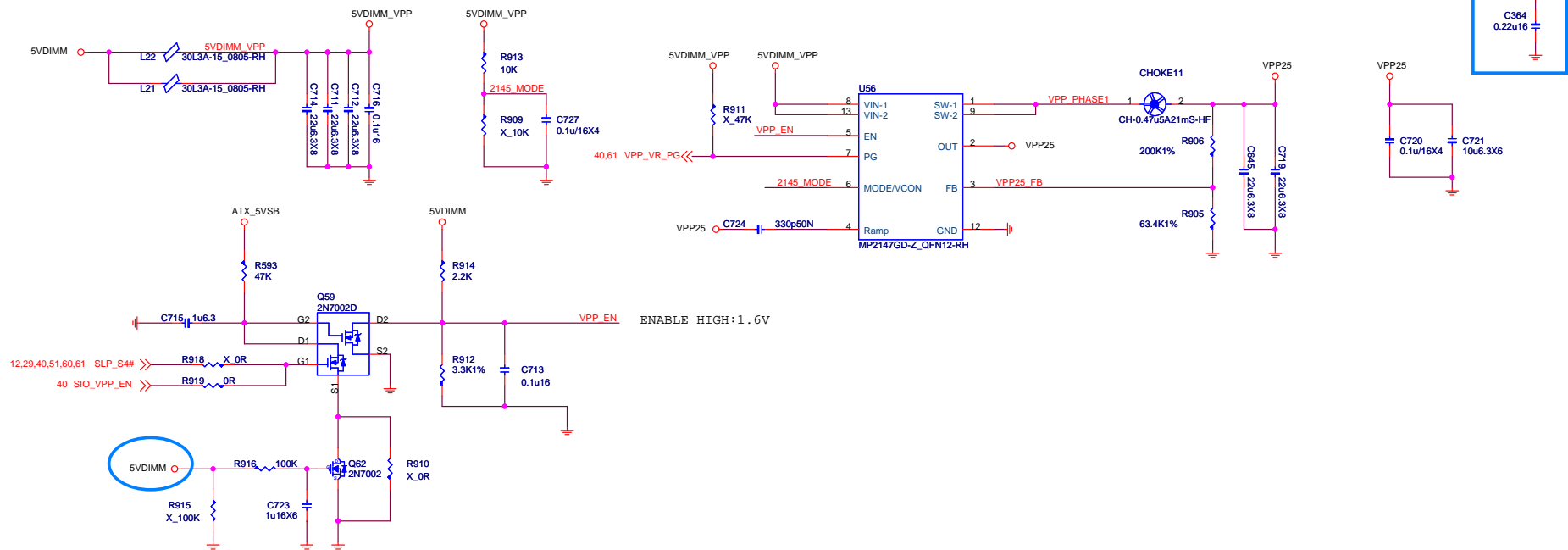
MS-7A59

Size Custom	Document Description CPU PWR_ST/PLL	Rev 1.1
Date: Monday, September 26, 2016		Sheet 60 of 70

Size Custom	Document Description DDR4 Power-RT8125C	Rev 1.1
Date: Monday, September 26, 2016		Sheet 61 of 70

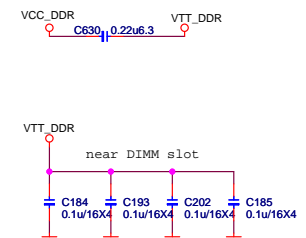
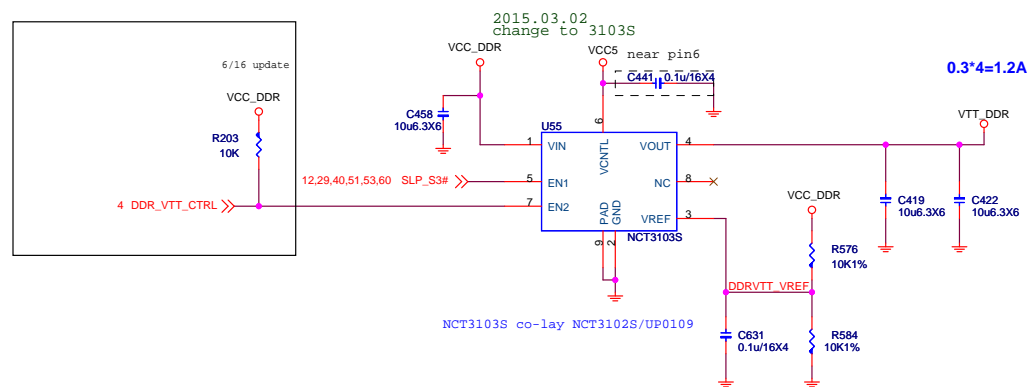
4DIMM :2.84A FOR DDR VPP2.5V

VPP25 Power
2.5V; 2.24A



To make sure VPP EN after 5VDIMM stable

DDR VTT Power



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PCH_1VSB

1.0V; 11.83A

OCP = 17.745A

Rocset = $1.5 * I_{max} * R_{dson(1ow)} / I_{ocset}$
 = $1.5 * 11.83 * 4.6mohm / 10uA$
 = 8.16K

Rocs:7.87K,OCP:
 D03-4C05N03-005 : 15.74A
 D03-632BA0C-N03 : 17.1A
 use UBIQ MOS need Check

Rdson(1ow)4.5V
 D03-3116M00-U47 : 3.6 mohm
 D03-632BA0C-N03 : 4.6mohm
 D03-3056M00-U47 : 6.2mohm

1504 change to 8125 I32-8125E0C-R11

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

$$I_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

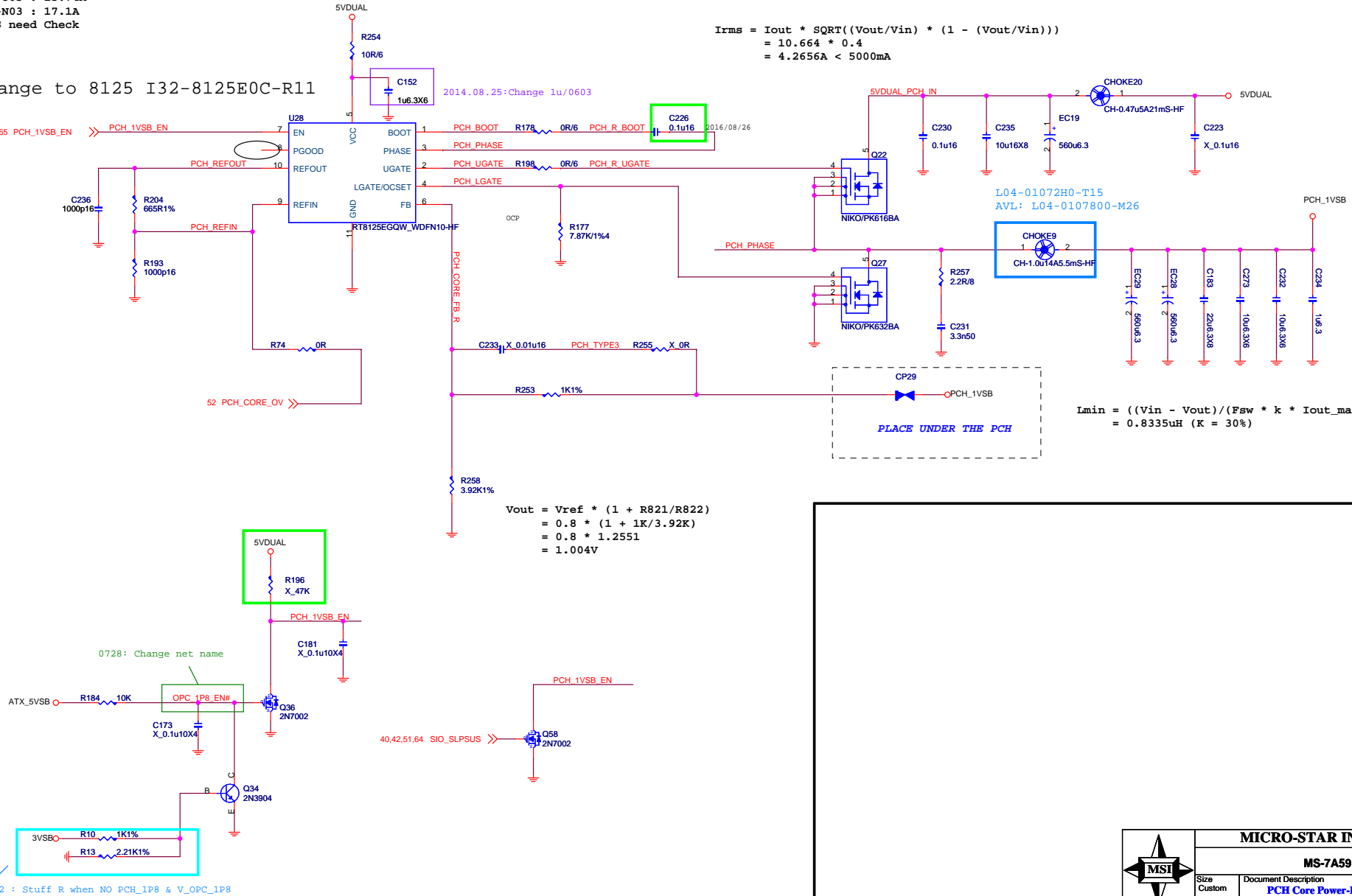
$$= 0.8335uH (K = 30\%)$$

$$V_{out} = V_{ref} * (1 + R_{821}/R_{822})$$

$$= 0.8 * (1 + 1K/3.92K)$$

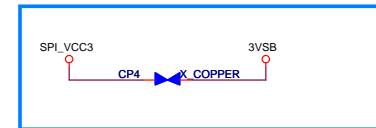
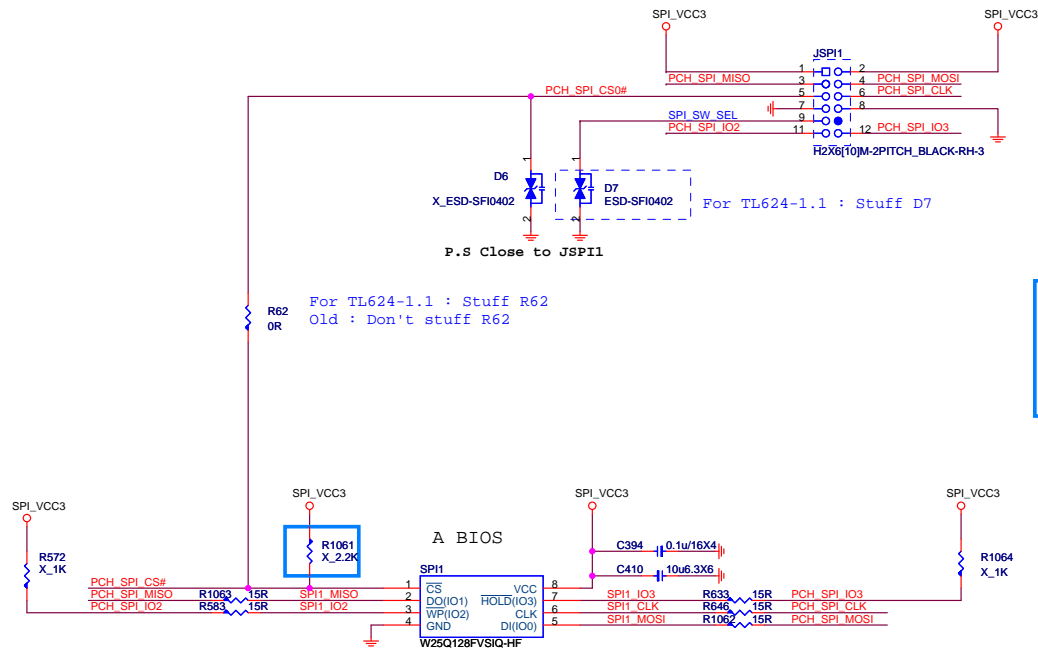
$$= 0.8 * 1.2551$$

$$= 1.004V$$

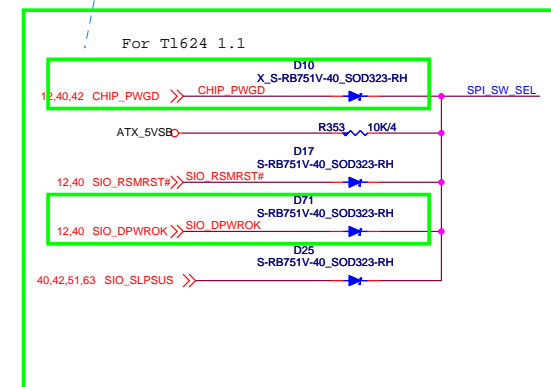


PLACE UNDER THE PCH

0902 : Stuff R when NO PCH_1P8 & V_OPC_1P8



Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.



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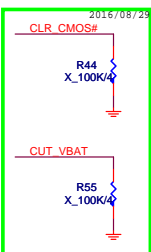
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Co-Lay NOT USE U1 , R150 STUFF

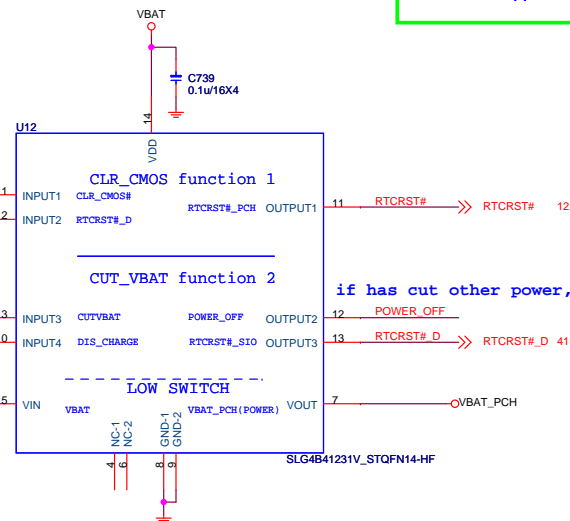
RTCRST# R150 X OR/4 RTCRST# D

If STUFF R150 Please Check RTCRST# Double Pull High

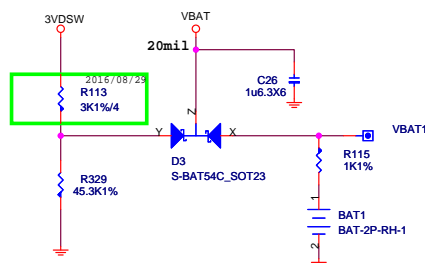
20160629



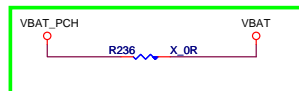
if has discharge function R232 NC.



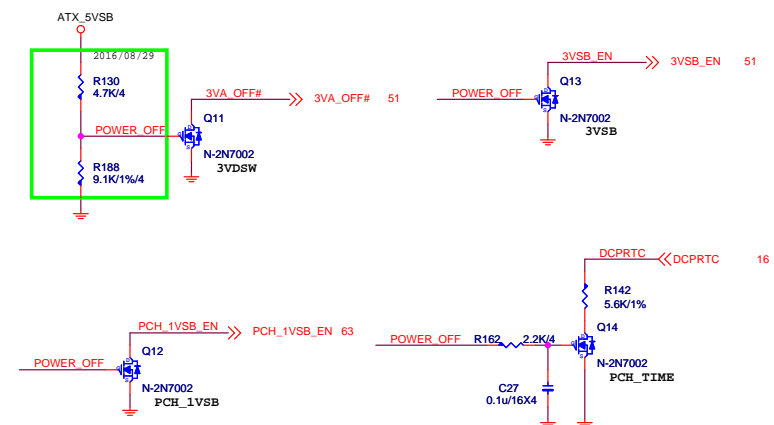
VBAT



Co-Lay NOT U1 , Stuff R18



Co-Lay NOT USE U1 , ALL UNSTUFF



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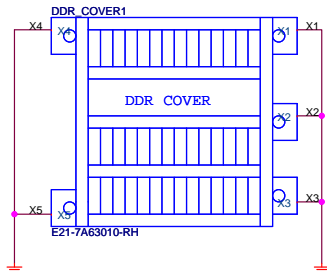
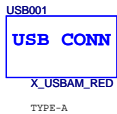
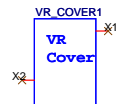
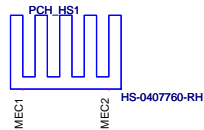
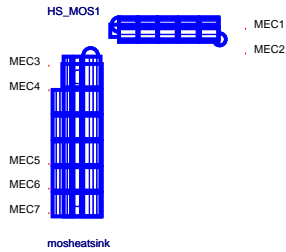
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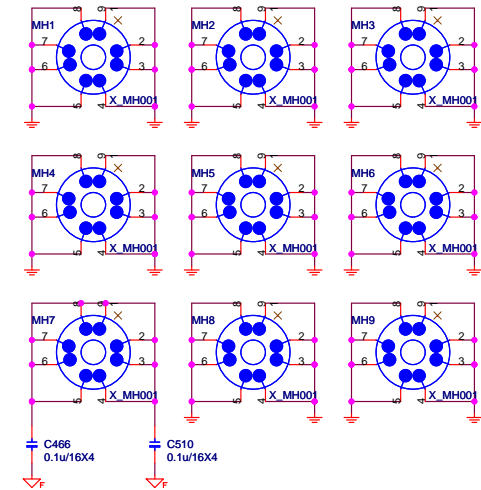
PCB



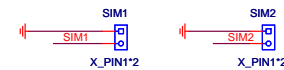
PD0-07A5911-G37
PD0-07A5911-E48



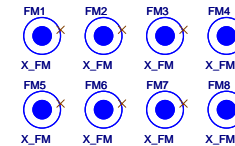
Mounting Holes



Simulation



Optical Fiducial Marks-120



Test point

